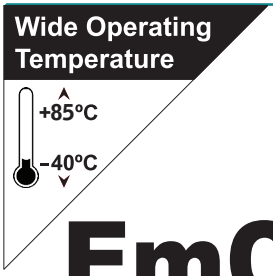


EmCORE-i90U2

3.5” Compact Board

User’s Manual

Version 1.0

2019.08

Revision History

Version	Release Time	Description
1.0	2019.08	Initial release

Contents

Preface

Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

Warning

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction

of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. Please consult your vendor before further handling.

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

https://www.arbor-technology.com
E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1. Packing List

Before starting with the installation, make sure the following items are shipped. If any item appears damaged or is missing, contact your vendor immediately:

1 x EmCORE-i90U2 3.5” Compact Board w/ Cooler

1 x Quick Installation Guide

1.2. Ordering Information

EmCORE-i90U2-WT-7600U	7th Generation Intel® Core™ i7-7600U 3.5” compact board
EmCORE-i90U2-WT-7300U	7th Generation Intel® Core™ i5-7300U 3.5” compact board
EmCORE-i90U2-WT-7100U	7th Generation Intel® Core™ i3-7100U 3.5” compact board

Optional Accessories

CBK-09-90U2-00	Cable kit 1 x Audio cable 1 x SATA cable 1 x SATA power cable 2 x USB 2.0 cables 4 x COM cables

1.3. Driver Installation (6.8A)

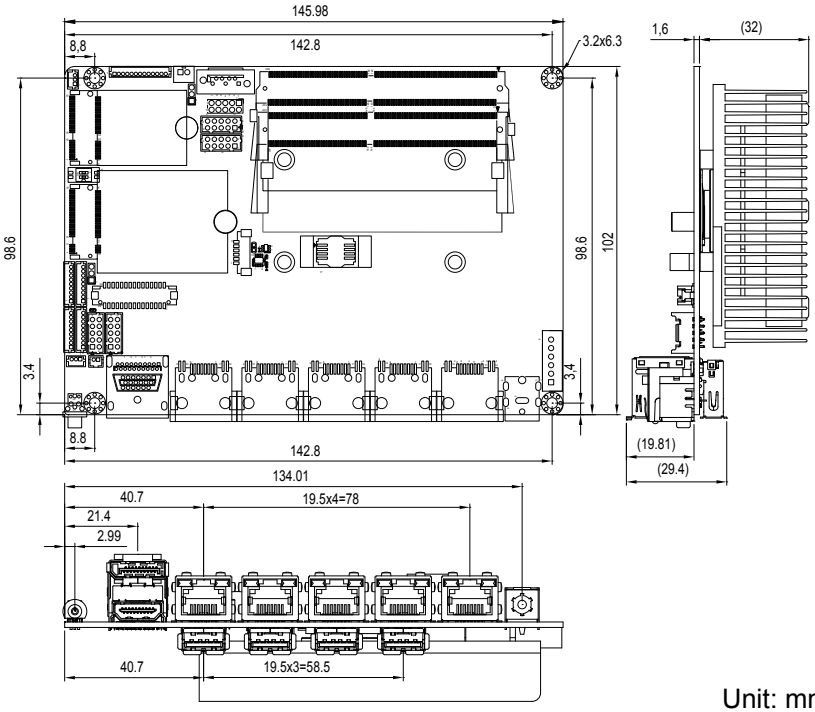
To install the drivers, please visit our website at **www.arbor-technology.com** and download the driver pack from the product page. The driver path is listed as below:

Driver	Path
Chipset	\EmETXe-i90x0\Chipset
Graphic	\EmETXe-i90x0\Graphic\win64
Audio	\EmETXe-i90x0\Audio\Win10_Win8.1_Win8_Win7_WHQLx64
Ethernet	\EmETXe-i90x0\Ethernet
ME	\EmETXe-i90x0\ME
RST	\EmETXe-i90x0\RST\SetupRST

1.4. Specifications

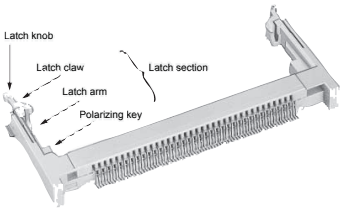
Form Factor	3.5" Compact Board
CPU	Soldered onboard 7th Gen. Intel® Core™ Processor i7-7600U 2.8GHz/ 3.4GHz, i5-7300U 2.6GHz/2.8GHz, i3-7100U 2.4GHz
Memory	2 x DDR4 SO-DIMM sockets, supporting 2133/1866MHz SDRAM up to 32GB
BIOS	AMI UEFI BIOS
TPM	Support TPM 1.2 SLB9660 & 2.0 SLB9665 function onboard (OEM request)
Watchdog Timer	1~255 levels reset
Super I/O	Fintek F81866
USB Port	4 x USB 3.0/2.0 ports 4 x USB 2.0 ports
Serial Port	4 x RS-232/422/485 selectable
Expansion	1 x M.2 E-key (2230) socket for Wi-Fi module
	1 x NANO SIM socket
	4 x PCIe x1 lanes or 1 x PCIe x4 with FFC connector (OEM request)
Storage	1 x Serial ATA port with 600MB/s HDD transfer rate
	1 x M.2 B-key (2242) socket for SATA SSD or LTE, depending on module
Ethernet Chipset	1 x Intel® i219LM PCIe PHY controller
	4 x Intel® i210IT PCIe GbE controllers supporting 802.3af PoE
Digital I/O	8-bit Programmable
Audio	Realtek® ALC269 5.1 Channel HD Audio CODEC, Mic-in/ Line-in/ Line-out
Graphic Chipset	Integrated Intel® HD Graphics 620
Graphic Interface	Dual Channel 24-bit LVDS
	1 x DisplayPort 1.2
	1 x HDMI 1.4 port
OS Support	Windows 10 64-bit, Linux Ubuntu
Power Requirement	9~15V or 15~36V DC-In (configurable via DIP switch)
Power Consumption	19V, 3.16A (i7-7600U, full loading w/ PoE) 19V, 3.15A (i5-7300U, full loading w/ PoE)
Operating Temp.	-40 ~ 85°C (-40 ~ 185ºF)
Operating Humidity	10 ~ 95% @ 85°C (non-condensing)
Dimensions (L x W)	146 x 102 mm (5.7" x 4.0")

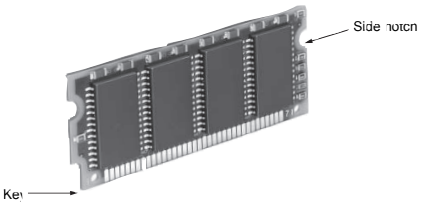
1.5. Board Dimensions



Unit: mm

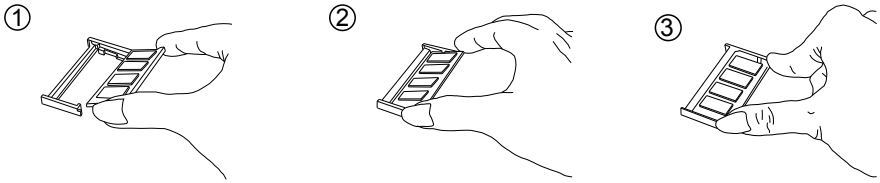
1.6 Installing the Memory





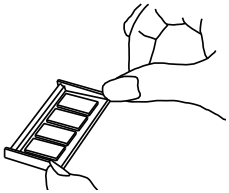
To install the Memory module, locate the Memory SO-DIMM slot on the board and perform as below:

1. Adjust the socket polarizing key and the board key to the same direction.
2. Insert the board obliquely. Moreover, lay the board in parallel to the opening at angle of 20^{o} to 30^{o}, and softly insert the board so as to hit the socket bottom. Stopping insertion halfway will result in improper insertion.
3. Applying the board side notch in parallel to the socket bottom so that the board position cannot be displaced, press the board side notch up, and fix it to the latch portion at both socket edges. Press the board side notch, and release the notch with a snap “click” tone, if the printed board exceeds the latch claw head.



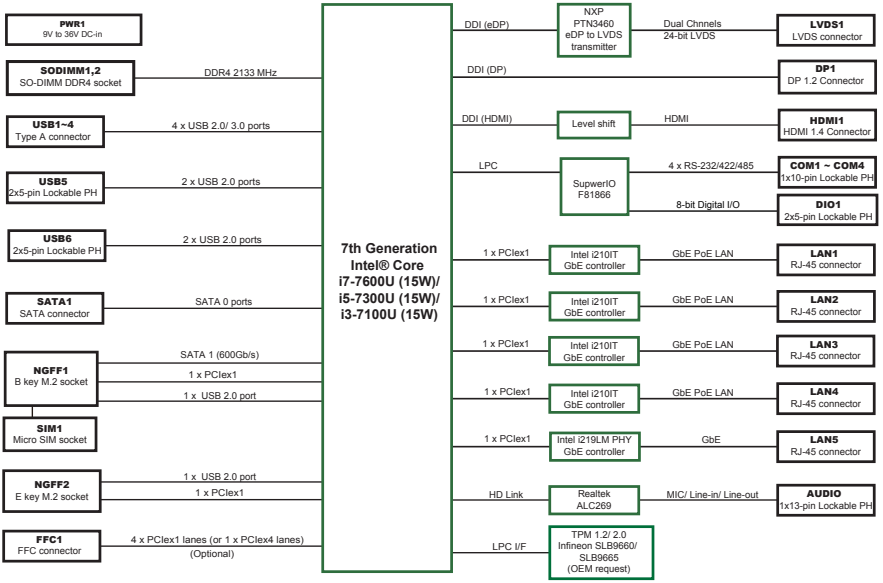
Procedures for board extraction

Apply the thumb nail to the latch knob at both socket edges. Forcibly widen the latch knobs to right and left ways, and release the latch. Then draw the board out along an angle where the board is raised.



Chapter 2
Installation

2.1. Block Diagram



2.2. Jumpers & Connectors Quick Reference

2.2.1 Jumpers

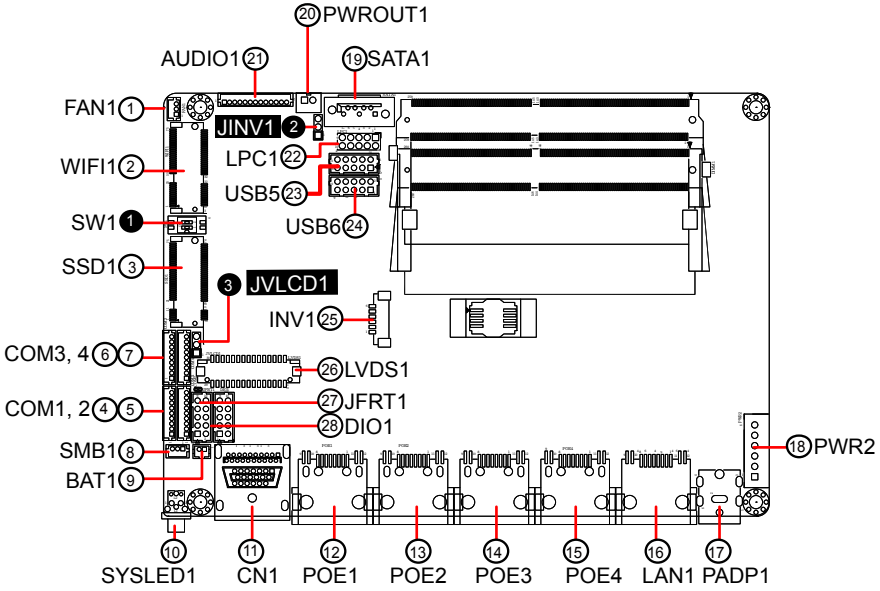
Jumper	Description
❶SW1	Power mode selection
❷JINV1	LCD inverter voltage selection
❸JVLCD1	LCD panel voltage selection

2.2.2 Connectors

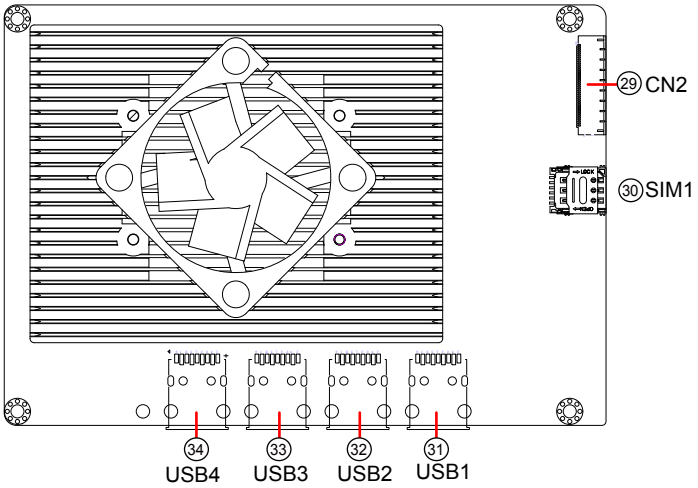
Connector	Description
①FAN1	CPU fan connector
②WIFI1	M.2 E-Key socket
③SSD1	M.2 B-Key socket
④~⑦COM1-4	Serial port connectors
⑧SMB1	SMBus connector
⑨BAT1	Battery connector
⑩SYSLED1	Power button & power on indicator
⑪CN1	DisplayPort & HDMI connector
⑫~⑮POE1~4	PoE connectors
⑯LAN1	GgE connector
⑰PADP1	9-36V DC power input connector (Option 1)
⑱PWR2	9-36V DC power input connector (Option 2)
⑲SATA1	Serial ATA connector
⑳PWROUT1	SATA power connector
㉑AUDIO1	Audio connector
㉒LPC1	Low pin count connector (for internal test)
㉓㉔USB5, 6	USB 2.0 connectors
㉕INV1	LCD inverter connector
㉖LVDS1	LVDS LCD panel connector
㉗JFRT1	Front-panel connector
㉘DIO1	Digital I/O connector
㉙CN2	1x PCIe x4 or 4 x PCIe x1 FPC connector (OEM request)
㉚SIM1	NANO SIM card socket
㉚~㉞USB1~4	USB 3.0 connectors

2.3. Jumpers & Connectors Location

Board Top



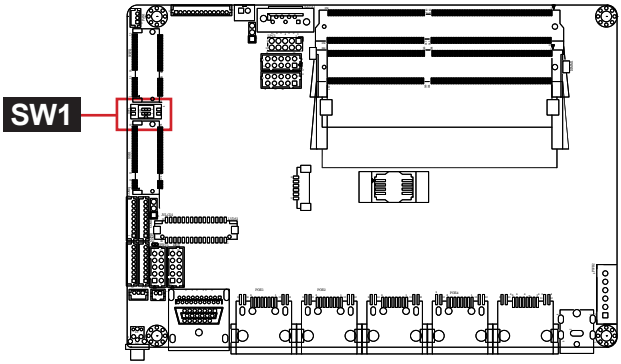
Board Bottom



2.3.1. Jumpers

❶ SW1: Power mode selection
Caution: When setting this jumper, make sure the motherboard is disconnected from the power

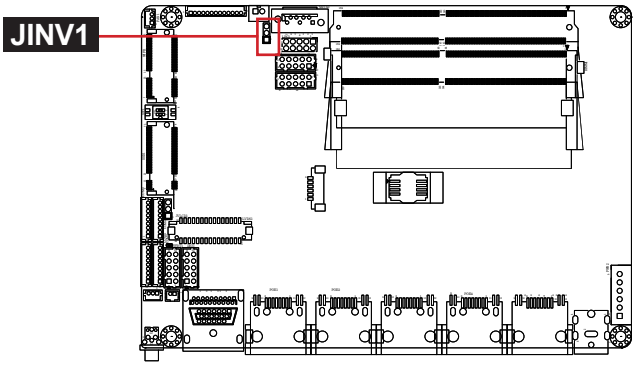
Mode	Description
Pin 1	**Input & LVDS inverter power selection**
On	15~36V power input When JINV1 = 1-2, INV1 Pin 1, 2 = 12V
Off	9~15V power input (default) When JINV1 = 1-2, INV1 Pin 1, 2 = 6.8V
Pin 2	**AT/ATX power mode selection**
On	AT mode
Off	ATX mode (default)



❷ JINV1: LCD inverter voltage selection

Jumper type: 2.00mm pitch 1x3-pin header

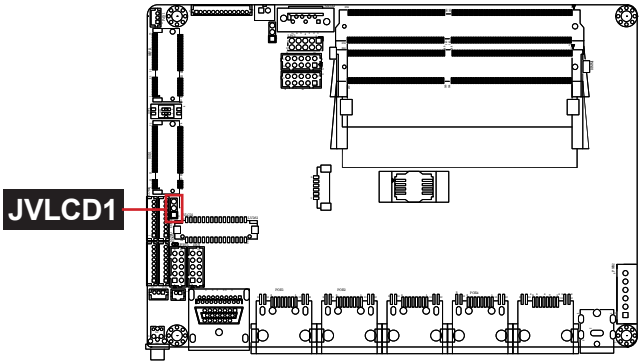
Pin	Description	
1-2	+12V, when SW1 Pin1 = On (default) +6.8V, when SW1 Pin1 = Off	
2-3	+5V	



❸ JVLCD1: LCD panel voltage selection

Jumper type: 2.00mm pitch 1x3-pin header

Pin	Description	
1-2	+5V	
2-3	+3.3V (default)	

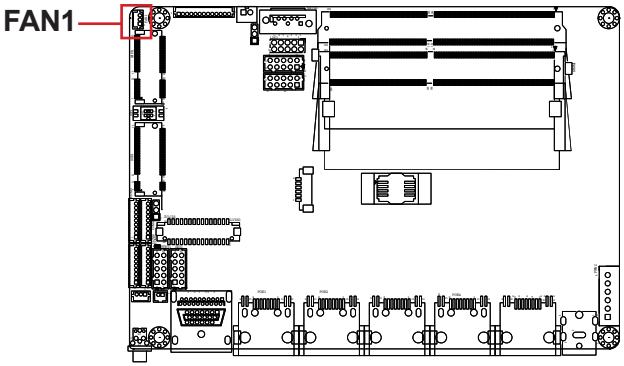


2.3.2. Connectors

①FAN1: CPU Fan Connector

Connector type: 1.25mm pitch 1x3-pin wafer connector

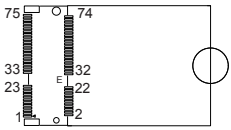
Pin	Description
1	GND
2	VCC
3	RPM



②WIFI1: M.2 E-Key socket

Connector Type: M.2 socket for E-Key 22x30 type to support WiFI module

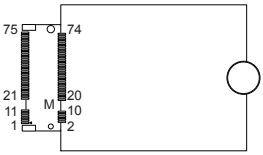
The pin assignments conform to the industry standard.

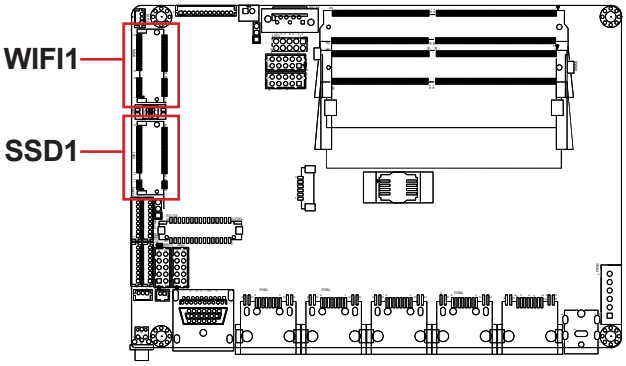


③SSD1: M.2 B-Key socket

Connector Type: M.2 socket for B-Key 22x42 type to support SATA SSD or LTE depending on module

The pin assignments conform to the industry standard.

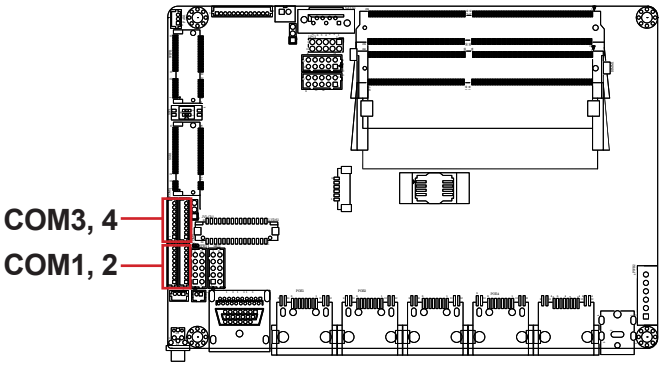




④⑤⑥⑦COM1-4: RS-232/422/485 Serial port connectors (mode selection via BIOS)

Connector type: 1.25mm pitch 1x9-pin wafer connector

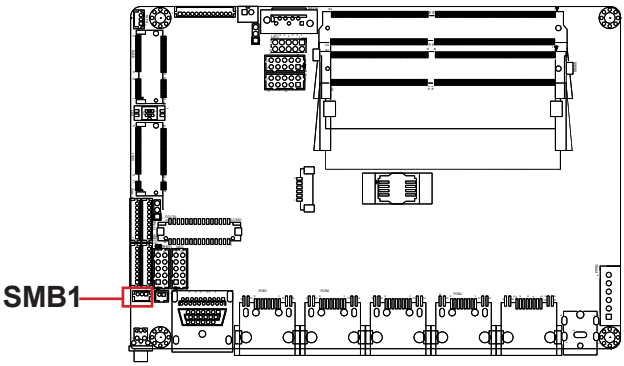
Pin	Description		
	RS-232	RS-422	RS-485
1	XDCD#	TX-	Data-
2	XDSR#		
3	XRXD	TX+	Data+
4	XRTS#		
5	XTXD	RX+	
6	XCTS#		
7	XDTR#	RX-	
8	XRI#		
9	GND		



⑧SMB1: SMBus Connector

Connector type: 1.25mm pitch 1x3-pin wafer connector

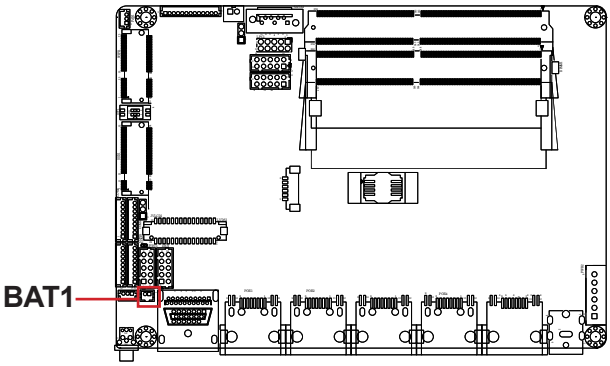
Pin	Description
1	SM_CLK
2	SM_DATA
3	GND



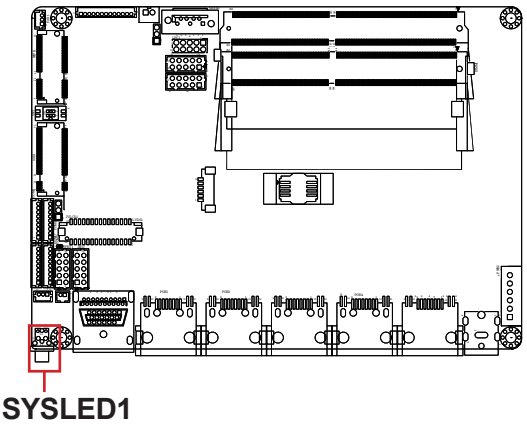
⑨BAT1: Battery connector

Connector type: 1.25mm pitch 1x2 pin wafer connector

Pin	Description
1	GND
2	Battery Power



⑩SYSLED1: Power button & power on indicator



⑪CN1A: DisplayPort Connector

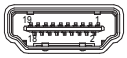
Connect the display device to the DisplayPort Connector

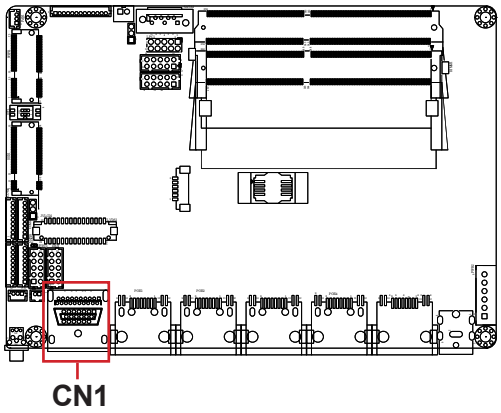
The pin assignments conform to the industry standard.

CN1B: HDMI 1.4 connector

Connector Type: 19-pin HDMI connector with flange

The pin assignments conform to the industry standard.

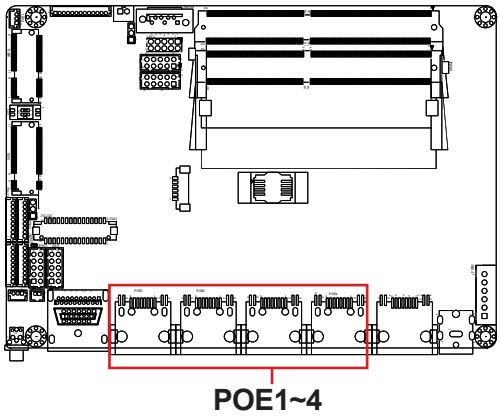




⑫~⑮POE1~4: PoE connector

Connector type: 10/100/1000Mbps fast Ethernet RJ-45 connector, supporting PoE, 802.3af

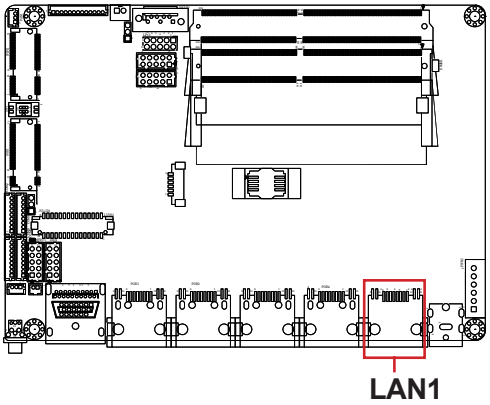
The pin assignments conform to the industry standard.



⑯LAN1: GbE connector

Connector type: 10/100/1000Mbps fast Ethernet RJ-45 connector

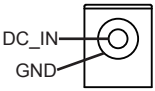
The pin assignments conform to the industry standard.



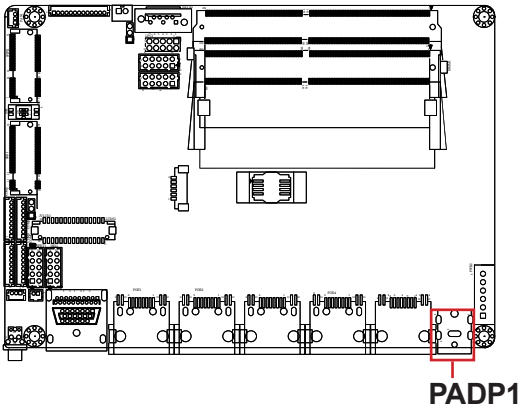
⑰PADP1: 9-36V DC power input connector (Option 1)

Connector type: DC power jack connector.

Pin	Description
1	DC_IN
2	GND



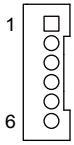
Caution: PADP1 and PWR2 cannot be used simultaneously.



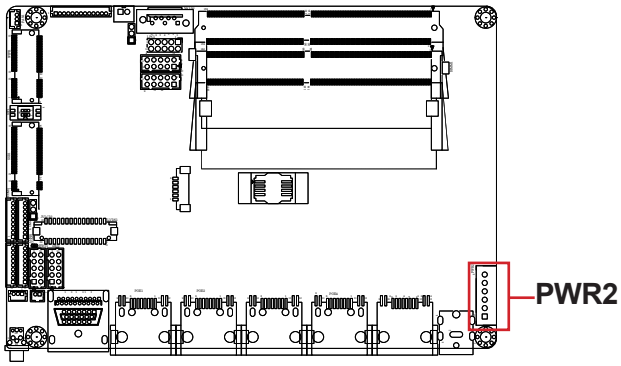
⑱ PWR2: 9-36V DC power input connector (Option 2)

Connector type: 2.5mm pitch 1x6 pin header

Pin	Description
1	DCIN
2	DCIN
3	DCIN
4	GND
5	GND
6	GND



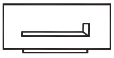
Caution: PADP1 and PWR2 cannot be used simultaneously.

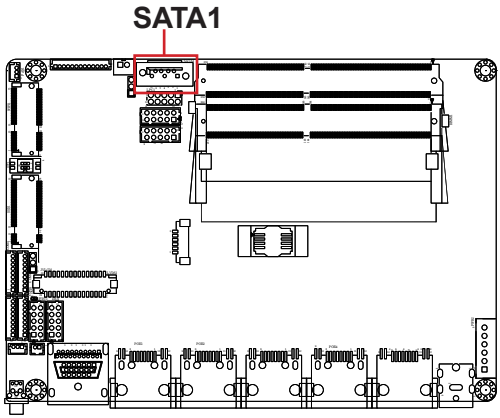


⑲ SATA1: Serial ATA connector

Connector type: SATA connector

The pin assignments conform to the industry standard.

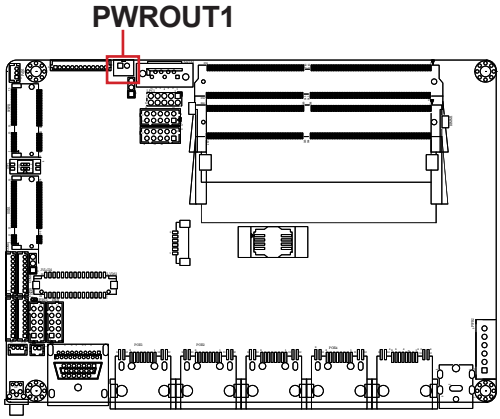




⑳ PWROUT1: SATA power connector

Connector type: 2.00mm pitch 1x2-pin wafer connector

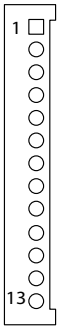
Pin	Description
1	+5VS
2	GND

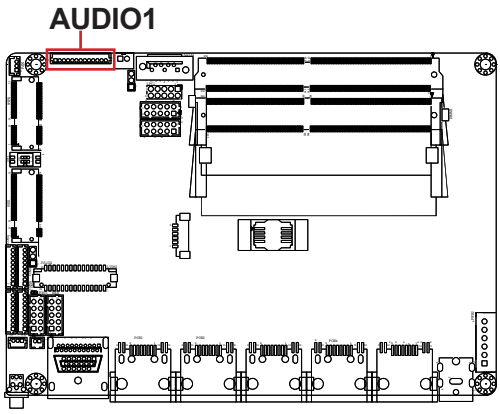


㉑ AUDIO1: Audio connector

Connector type: 1.25mm pitch 1x13-pin wafer connector

Pin	Description
1	LINL
2	LINR
3	LIN_JD
4	AGND
5	MICL
6	MICR
7	MIC_JD
8	AGND
9	LOUT-L
10	LOUT-R
11	FRONT_JD
12	AGND
13	NC

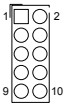


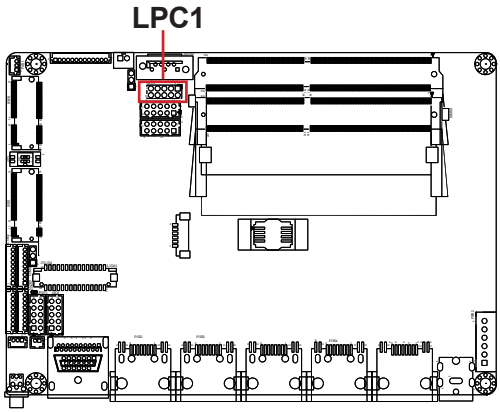


㉒LPC1: Low Pin Count Connector (for internal test)

Connector type: Onboard 2.00mm pitch 2x5 female pin header

Pin	Description	Pin	Description
1	CLK_LPC	2	GND
3	LPC_FRAME#	4	LPC_AD0
5	PLTRST#_BUFF	6	NC
7	LPC_AD3	8	LPC_AD2
9	+3.3VS	10	LPC_AD1



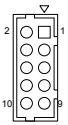


㉓㉔USB5, 6: USB 2.0 connectors

Connector type: 2.00mm pitch 2x5-pin wafer connector

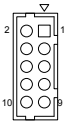
USB5

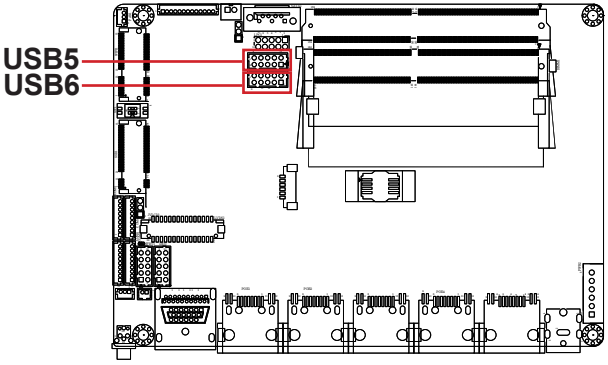
Pin	Description	Pin	Description
2	+5V_USB56	1	+5V_USB56
4	USBN6N	3	USBN5N
6	USBN6P	5	USBN5P
8	GND	7	GND
10	GND	9	GND



USB6

Pin	Description	Pin	Description
2	+5V_USB56	1	+5V_USB56
4	USBN8N	3	USBN7N
6	USBN8P	5	USBN7P
8	GND	7	GND
10	GND	9	GND

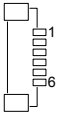


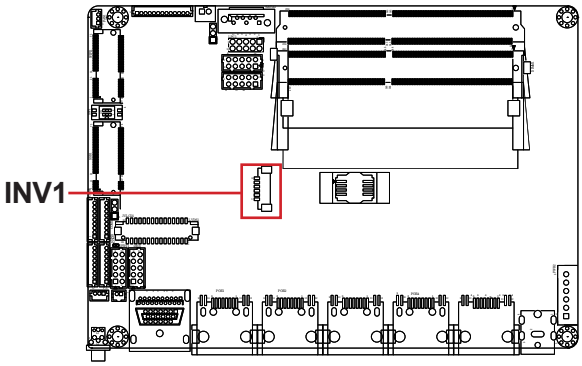


㉕ INV1: LCD inverter connector

Connector type: 1.25mm pitch 1x6-pin box wafer connector

Pin	Description
1	LVDS1_INV
2	LVDS1_INV
3	LVDS1_BKLT_EN
4	LVDS1_BKLT_CTRL
5	GND
6	GND

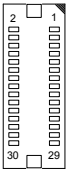


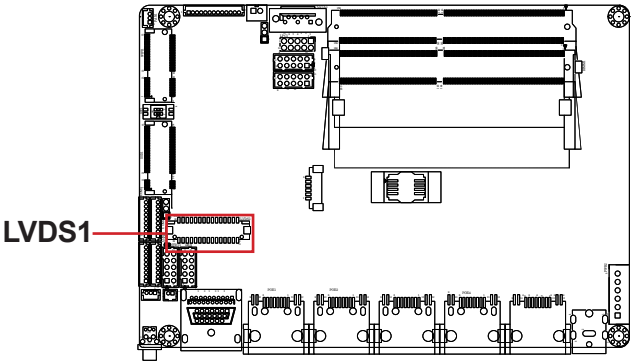


㉖ LVDS1: LVDS LCD panel connector

Connector type: ACES 1.25mm 87209-3040-06 connector that supports 24-bit dual channels.

Pin	Description	Pin	Description
2	VDD	1	VDD
4	TX2_CLK+	3	TX1_CLK+
6	TX2_CLK-	5	TX1_CLK-
8	GND	7	GND
10	TX2_D0+	9	TX1_D0+
12	TX2_D0-	11	TX1_D0-
14	GND	13	GND
16	TX2_D1+	15	TX1_D1+
18	TX2_D1-	17	TX1_D1-
20	GND	19	GND
22	TX2_D2+	21	TX1_D2+
24	TX2_D2-	23	TX1_D2-
26	GND	25	GND
28	TX2_D3+	27	TX1_D3+
30	TX2_D3-	29	TX1_D3-

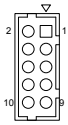


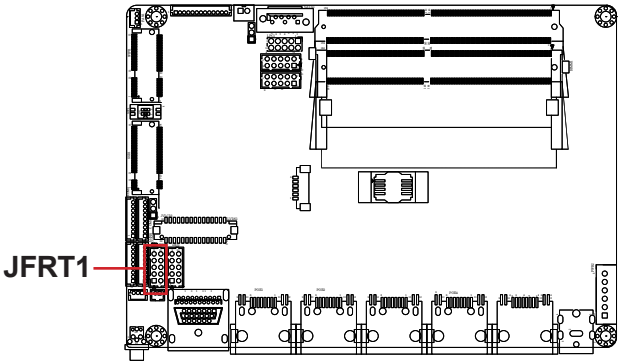


㉗ JFRT1: Front-panel connector

Connector type: 2.00mm pitch 2x5-pin wafer connector

Pin	Description	Pin	Description
2	HDD+	1	PWRLED+
4	HDD-	3	PWRLED-
6	GND	5	EC_PWRBTN_IN#
8	RSTBTNDB	7	GND
10	EX_SPKOUT+	9	EX_SPKOUT#

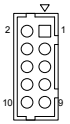


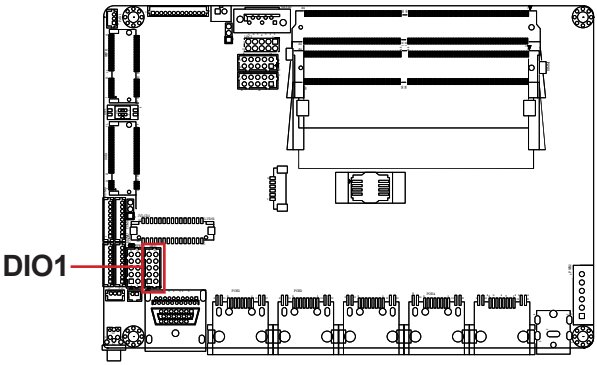


㉘ DIO1: Digital I/O Connector

Connector type: 2.00mm pitch 2x5-pin wafer connector

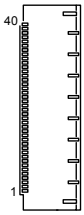
Pin	Desc.	Pin	Desc.
2	DIO1	1	DIO0
4	DIO3	3	DIO2
6	DIO5	5	DIO4
8	DIO7	7	DIO6
10	GND	9	+V5S



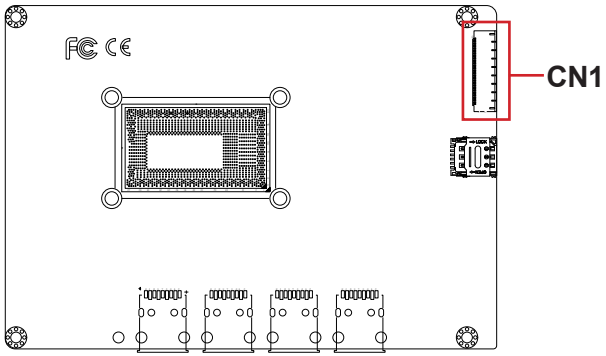


㉙ CN2: 1x PCIe x4 or 4 x PCIe x1 FPC Connector (OEM Request)

Connector type: FFC/FPC 1x 40P-pin connector



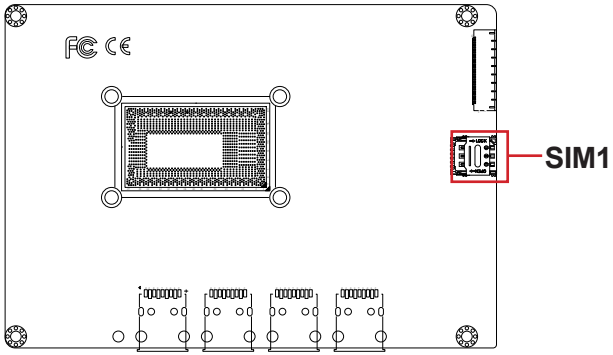
Pin	Description	Pin	Description
1	GND	21	PCIE_TXP12
2	PCIE_TXN9	22	GND
3	PCIE_TXP9	23	PCIE_RXN12
4	GND	24	PCIE_RXP12
5	PCIE_RXN9	25	GND
6	PCIE_RXP9	26	CLKOUT_PCIE_N4
7	GND	27	CLKOUT_PCIE_P4
8	PCIE_TXN10	28	GND
9	PCIE_TXP10	29	SMB_DATA_RESUME
10	GND	30	SMB_CLK_RESUME
11	PCIE_RXN10	31	GPP_C22_DIO_INT
12	PCIE_RXP10	32	+V5A
13	GND	33	PWRON_CTRL
14	PCIE_TXN11	34	CB_RESET#
15	PCIE_TXP11	35	RSTBTNDB
16	GND	36	EX_PWRBN_IN#
17	PCIE_RXN11	37	PCH_WAKE#
18	PCIE_RXP11	38	+5VA
19	GND	39	+5VA
20	PCIE_TXN12	40	GND



㉚ SIM1: NANO SIM card socket

Connector type: SMD,6P,1.27mm,H1.5 socket

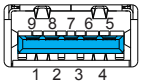
Pin	Description	Pin	Description
C1	VCC	C2	RST
C3	CLK	C5	GND
C6	VPP	C7	I/O

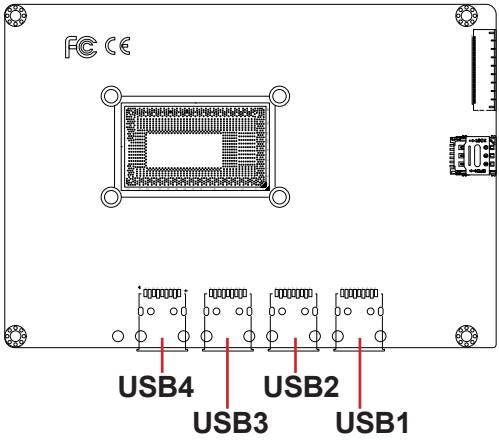


㉛ ~㉞ USB1~4: USB 3.0 connector

Connector type: USB 3.0/2.0 type-A connectors

The pin assignments conform to the industry standard.





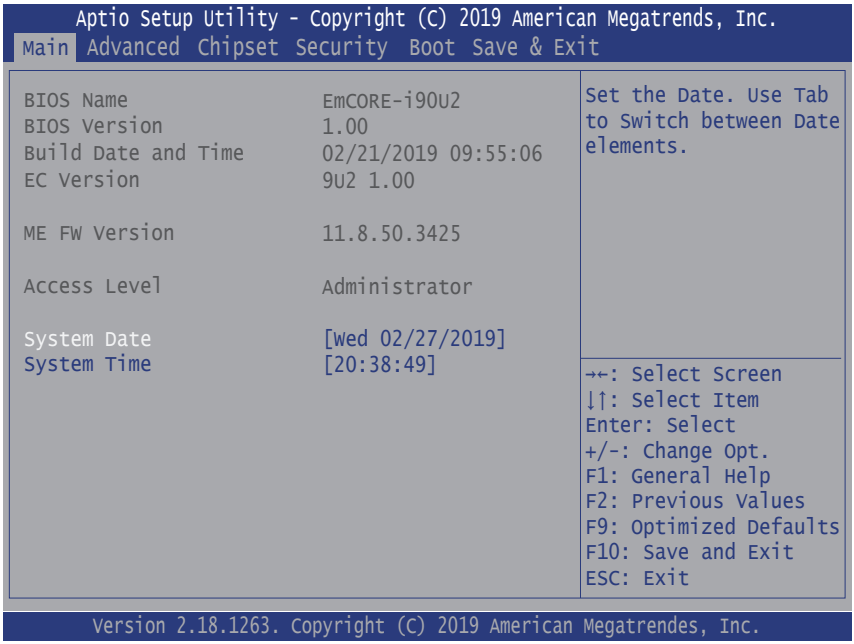
Chapter 3

BIOS

3.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **"Delete"** once the power is turned on.

The **Main Setup** screen lists the following information:



Setting	Description
System Date	Set the system date. Use Tab to switch between Data elements. Note that the 'Day' automatically changes when you set the date. ► The date format is: **Day:** Sun to Sat **Month:** 1 to 12 **Date:** 1 to 31 **Year:** 1998 to 2099

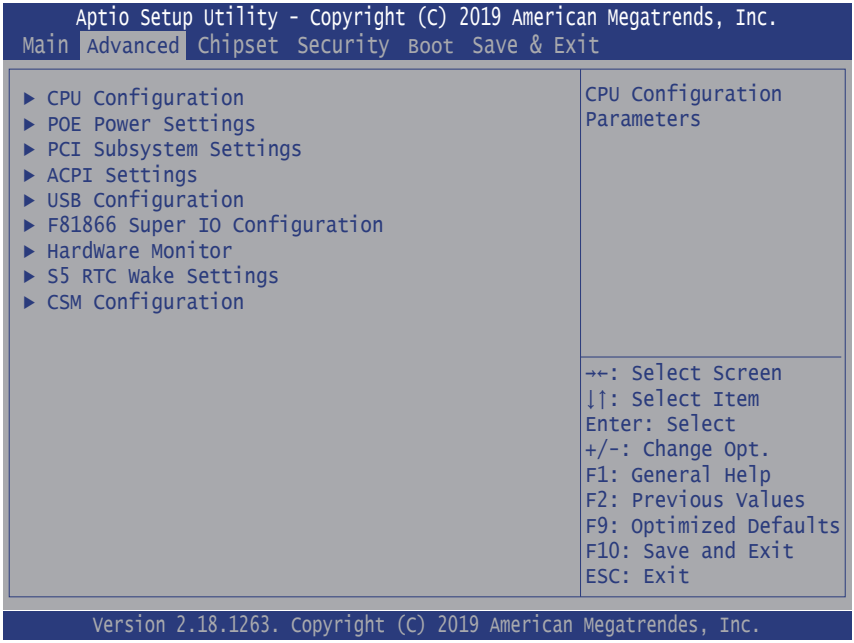
System Time	Set the system time. Use Tab to switch between Time elements. ► The time format is: **Hour:** 00 to 23 **Minute:** 00 to 59 **Second:** 00 to 59

Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

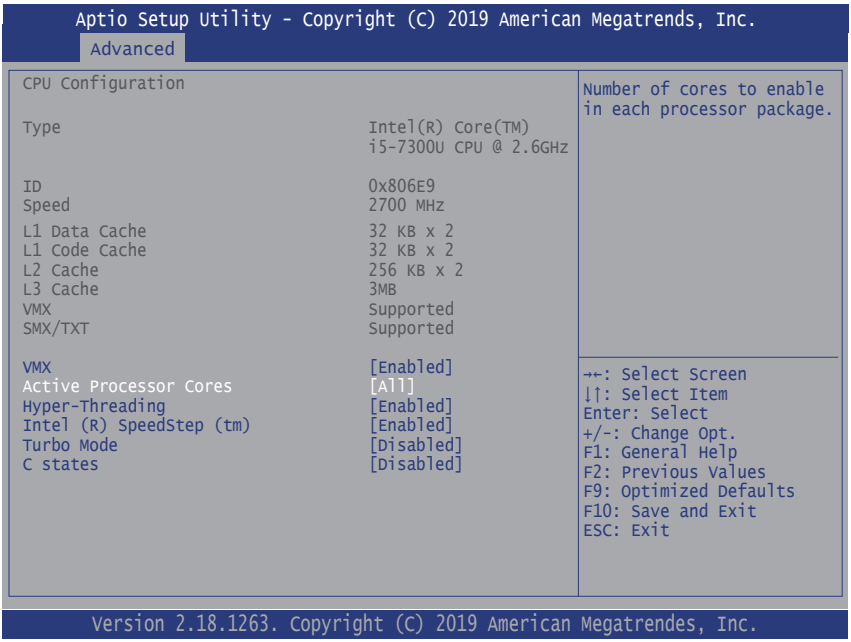
Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down / -	Decrease the numeric value on a selected setup item / make change
F1	Activate “General Help” screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm)

3.2 Advanced



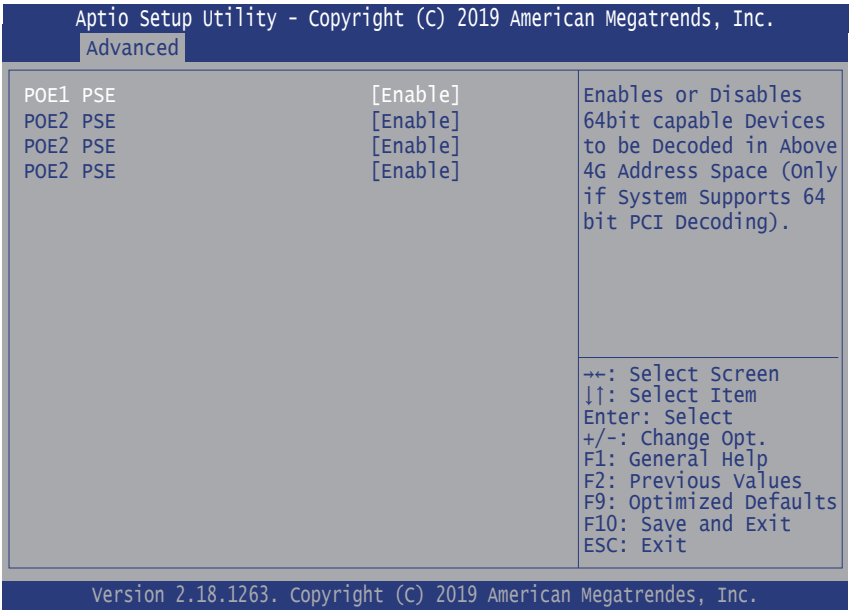
Setting	Description
CPU Configuration	See section 3.2.1 CPU Configuration on page 35
POE Power Settings	See section 3.2.2 POE Power Settings on page 36
PCI Subsystem Settings	See section 3.2.3 PCI Subsystem Settings on page 37
ACPI Settings	See section 3.2.4 ACPI Settings on page 38
USB Configuration	See section 3.2.5 USB Configuration on page 39
F81866 Super IO Configuration	See section 3.2.6 F81866 Super IO Configuration on page 41
Hardware Monitor	See section 3.2.7 Hardware Monitor on page 42
S5 RTC Wake Settings	See section 3.2.8 S5 RTC Wake Settings on page 43
CSM Configuration	See section 3.2.9 CSM Configuration on page 44

3.2.1 CPU Configuration



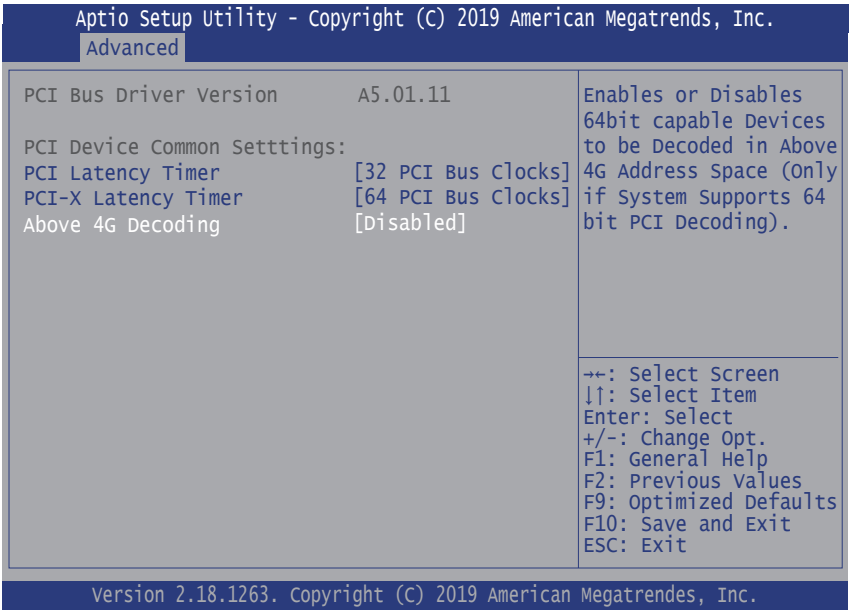
Setting	Description
VMX	**Enable** (default)/**Disable** Intel virtualization technology.
Active Processor Cores	Number of cores to enable in each processor package. ► Options: **All** (default) and **1**
Hyper-threading	**Enabled** (default) for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and **Disabled** for other OS (OS not optimized or Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
Intel (R) Speed Step (tm)	**Enable** (default)/**Disable** Intel SpeedStep
Turbo Mode	Only available when Intel Speed Step is **Enabled**. **Enable**/**Disable** (default) Turbo Mode
C States	**Enable** /**Disable** (default) CPU C States

3.2.2 POE Power Settings



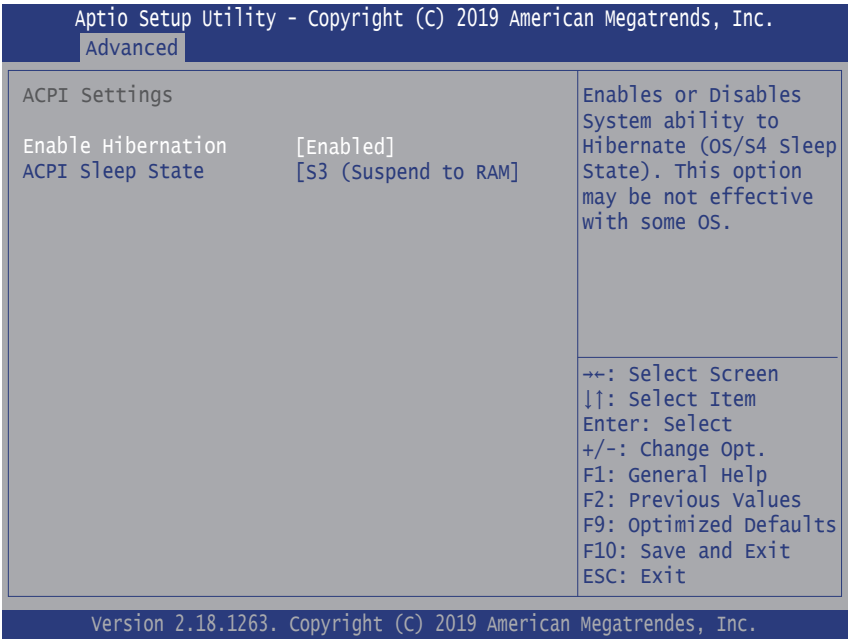
Setting	Description
PoE 1~4 PSE	**Enable**(default)/**Disable** POE power sourcing equipment (PSE) setting.

3.2.3 PCI Subsystem Settings



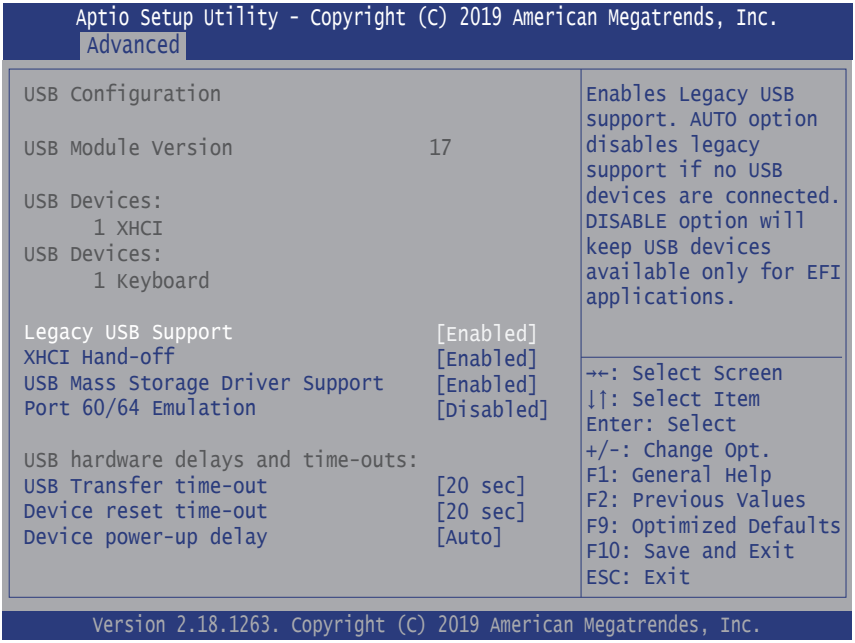
Setting	Description
PCI Latency Timer	Value to be programmed into PCI Latency Timer Register. ► **32** (default), **64**, **96**, **128**, **160**, **192**, **224** and **248 PCI Bus Clocks**.
PCI-X Latency Timer	Value to be programmed into PCI-X Latency Timer Register. ► **32**, **64** (default), **96**, **128**, **160**, **192**, **224** and **248 PCI Bus Clocks**.
Above 4G Decoding	**Enable**/**Disable** (default) 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

3.2.4 ACPI Settings



Setting	Description
Enable Hibernation	**Enable** (default) or **Disable** System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed. ► Options: **Suspend Disabled** and **S3 (Suspend to RAM)** (default).

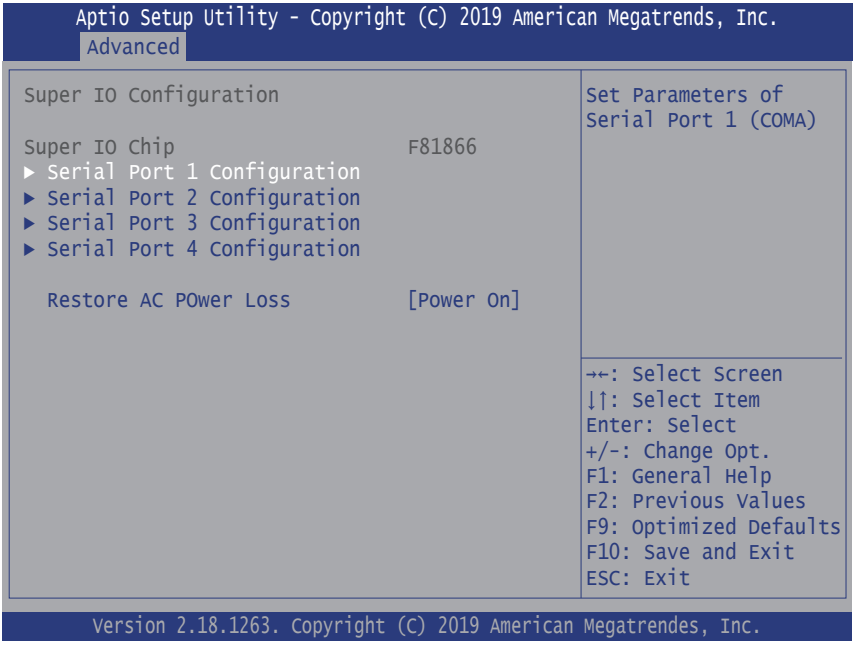
3.2.5 USB Configuration



Setting	Description
Legacy USB Support	Sets legacy USB support. ► Options: **Enabled** (default), **Disabled** and **Auto**. **AUTO** option disables legacy support if no USB devices are connected. **Disable** option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enable** (default) or **Disable** XHCI Hand-off This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	**Enable** (default) or **Disable** USB Mass Storage Driver Support.

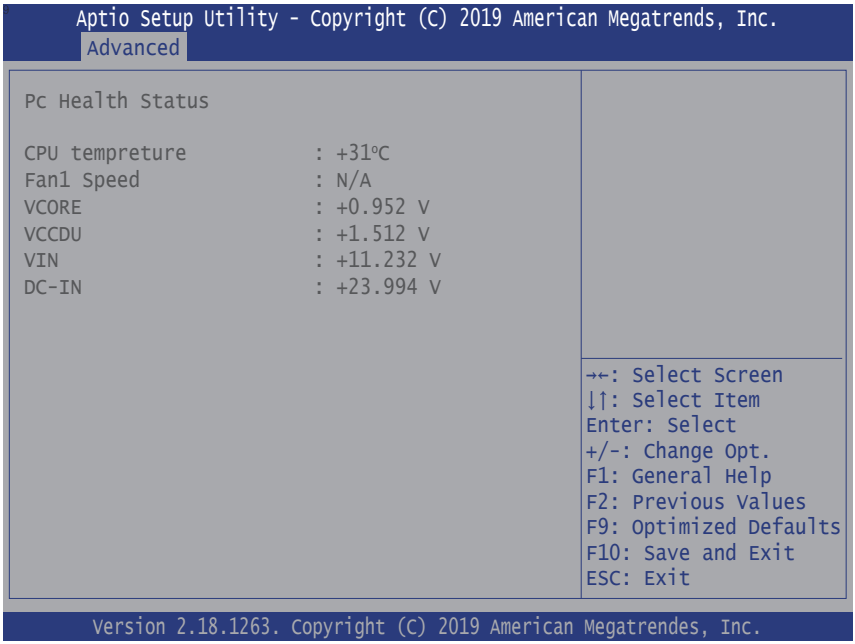
Port 60/64 Emulation	**Enable** or **Disable** (default) I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy suppot for non-USB aware OSes.
USB hardware delay and time-out	
USB Transfer time-out	Use this item to set the time-out value for control, bulk, and interrupt transfers. ▸ Options available are: **1 sec, 5 sec, 10 sec, 20 sec** (default)
Device reset time-out	Use this item to set USB mass storage device start unit command time-out. ▸ Options available are: **10 sec, 20 sec** (default)**, 30 sec, 40 sec**
Device power-up delay	Use this item to set maximum time the device will take before it properly reports itself to the host controller. ▸ Options available are: **Auto** (Default): 'Auto' uses default value: for a root port it is 100 ms, for a hub port the delay is taken from hub descriptor. **Manual**: Select **Manual** you can set value for the following sub-item: '**Device Power-up delay in seconds**', the delay range in from 1 to 40 seconds, in one second increments.

3.2.6 F81866 Super IO Configuration



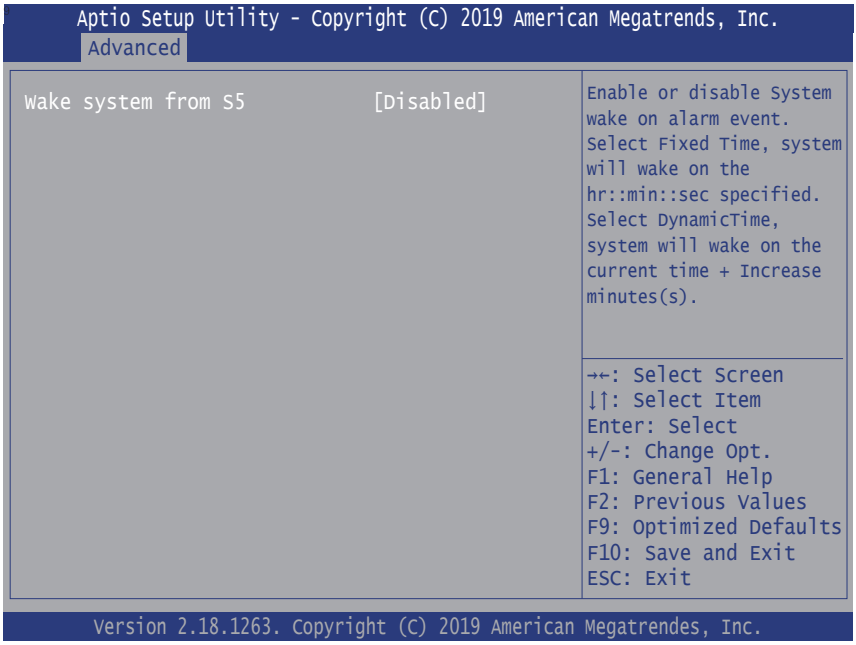
Setting	Description
Serial Port 1~4 Configuration	**Serial Port** **Enable** (default) or **Disable** Serial Port (COM). **COM Mode Settings** Select the COM port mode: ► Options for Serial Port 1: **RS-422**; **RS-422 with termination resistor**; **RS-485 with termination resistor**; **RS-232** (default); **RS-485**;
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure. ► Options: **Power Off**, **Power On** (default) and **Last State**.

3.2.7 Hardware Monitor



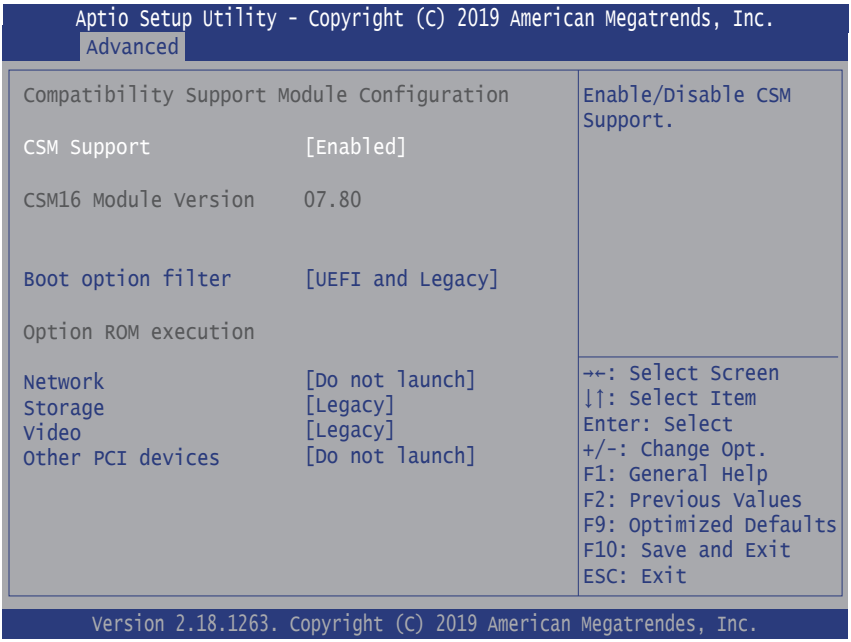
Access this submenu to monitor the hardware status.

3.2.8 S5 RTC Wake Settings



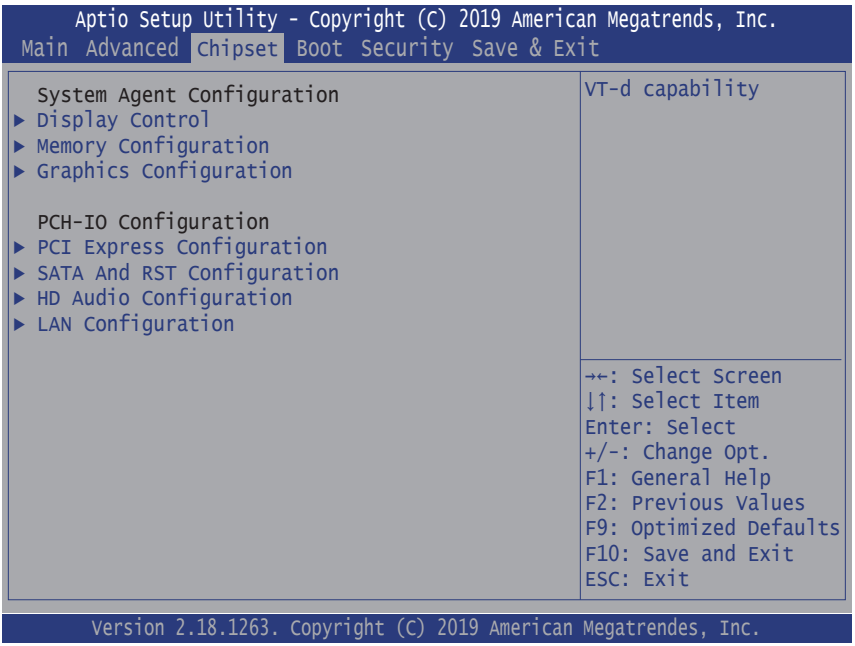
Setting	Description
Wake System from S5	**Enable** or **Disable** (default) system wake on alarm event. ► Options available are: **Disabled** (default): **Fixed Time:** System will wake on the hr::min::sec specifiedc. **DynamicTime:** If selected, you need to set **Wake up minute increase** from 1 - 5. System will wake on the current time + increase minute(s).

3.2.9 CSM Configuration



Setting	Description
CSM Support	**Enable** (default) or **Disable** CSM Support.
Boot option filter	Control the Legacy/UEFI ROMs priority. ► Options: **UEFI and Legacy** (default), **Legacy only** and **UEFI only**
Network	Control the execution of UEFI and Legacy PXE OpROM ► Options: **Do not launch** (default) **UEFI** and **Legacy**
Storage	Control the execution of UEFI and Legacy Storage OpROM ► Options: **Do not launch** and **Legacy** (default)
Video	Control the execution of UEFI and Legacy Video OpROM ► Options: **Do not launch** and **Legacy** (default)
Other PCI devices	Determines OpROM execution policy for devices other than Network, Storage, or Video ► Options: **Do not launch** (default), **UEFI** and **Legacy**

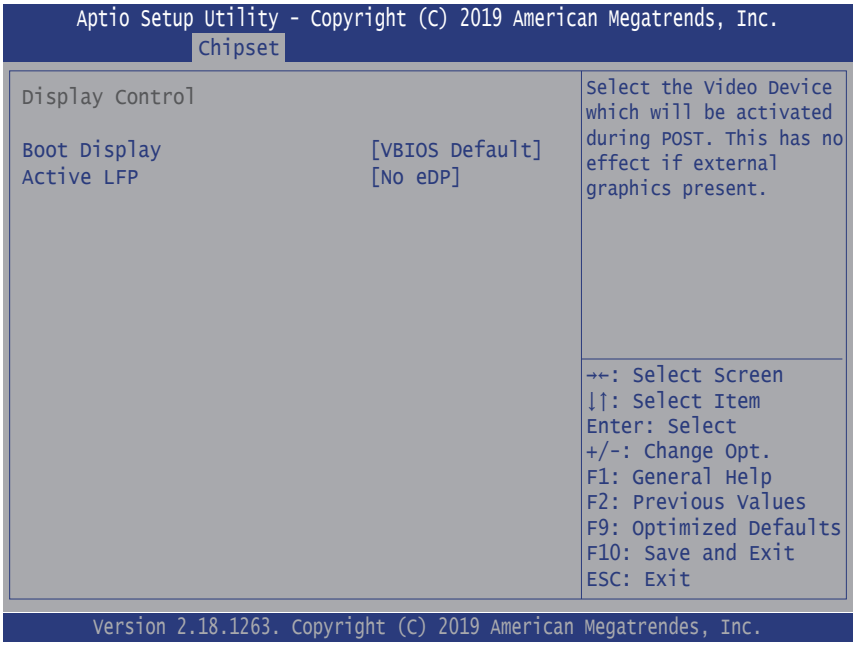
3.3 Chipset



Setting	Description
System Agent (SA) Configuration	
Display Control	See section 3.3.1 Display Control on page 47
Memory Configuration	See section 3.3.2 Memory Configuration on page 48
Graphics Configuration	See section 3.3.3 Graphics Configuration on page 49
PCH-IO Configuration	
PCI Express Configuration	See section 3.3.4 PCI Express Configuration on page 51
SATA And RST Configuration	See section 3.3.5 SATA And RST Configuration on page 52

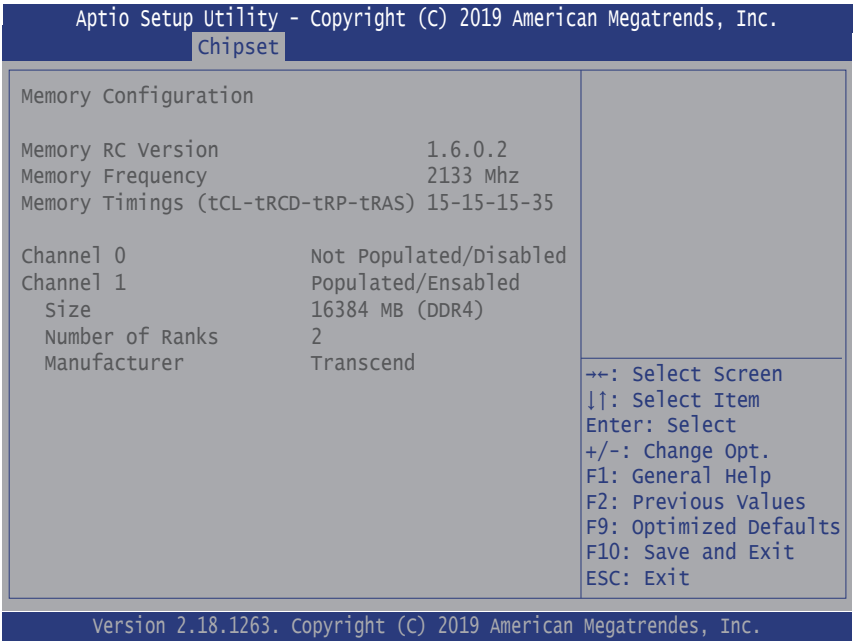
HD Audio Configuration	Control Detection of the HD-Audio device. ► Options available are: **Disabled**: HDA will be unconditionally disabled **Enabled**: HDA will be unconditionally Enabled **Auto** (default): HDA will be enabled if present, disabled otherwise.
LAN Controller	Enables/Disables onboard NIC. ► Options: **Enabled** (default) and **Disabled** If enabled, “Wake on LAN” option will be available to **Enable** (default) / **Disable** integrated LAN to wake the system. (the Wake On LAN cannot be disabled if ME is on at Sx state.)

3.3.1 Display Control



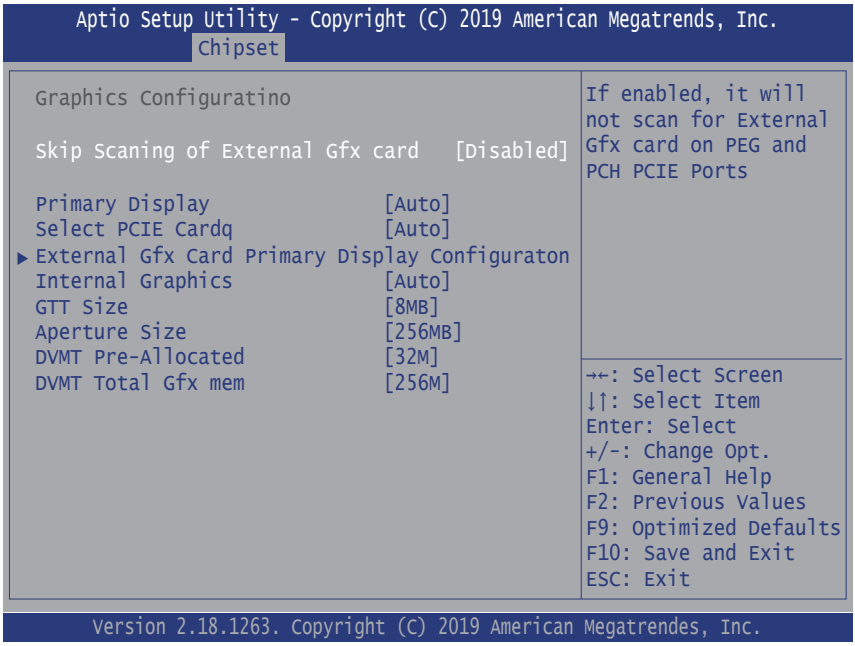
Setting	Description
VBIOS	Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display. ► Options: **VBIOS Default** (default), **LVDS**, **HDMI** and **DP1**.
Active LFP	Configuring LFP usage ► Options: **No eDP** (default) and **eDP Port-A**

3.3.2 Memory Configuration



Access this submenu to view the memory configuration.

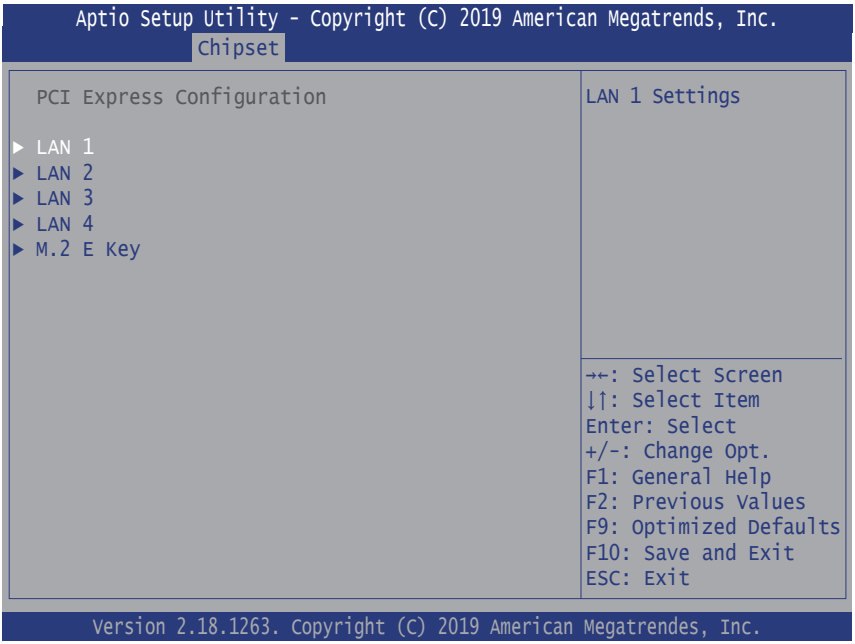
3.3.3 Graphics Configuration



Setting	Description
Skip Scaning of External Gfx Card	If enabled, it will not scan for external Gfx Card on PEG and PCH PCIE ports. ► Options: **Enable** and **Disable** (default)**.**
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx. ► Options: **Auto** (default), **IGFX**, **PEG**, **PCI** and **SG**
Select PCIE Card	Select the card used on the platform. Options: ► **Auto** (default): Skip GPIO based power enable to dGPU ► **ELK Creek 4**: DGPU power enable = ActiveLow ► **PEG EVal**: DGPU Power Enable = ActiveHigh

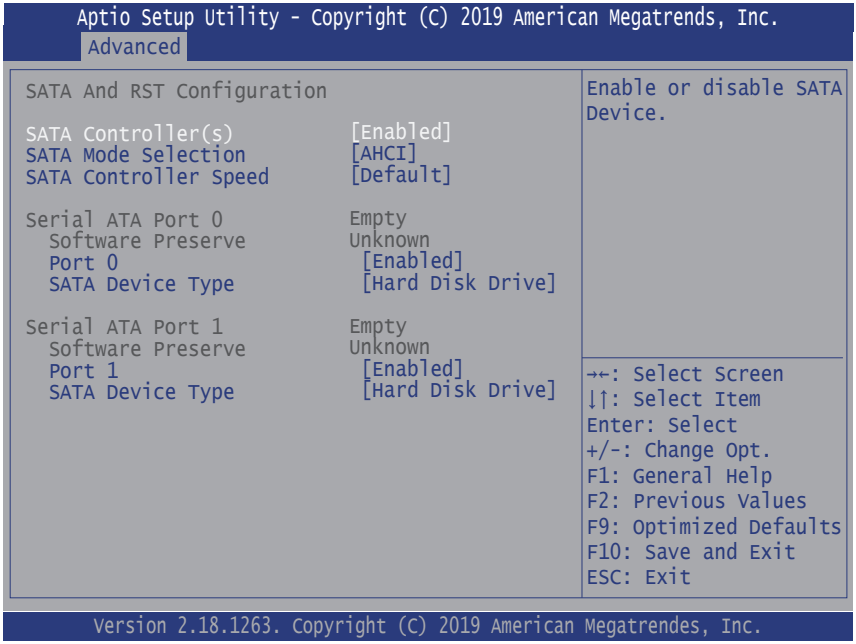
External Gfx Card Primary Display Configuraiton	**Primayr PEG:** Select the graphic device that should be Primary PEG. ► Options: **Auto**(default)**, PEG11** and **PEG12** **Primayr PCIE:** Select the graphic device that should be Primary PCIE. ► Options: **Auto**(default)**, PCIE1~18**
Internal Graphics	Keep IGFX enabled based on the setup options. ► Options: **Auto** (default), **Disabled** and **Enabled**
GTT Size	Select the GTT Size. ► Options: **2MB, 4MB** and **8MB** (default)**.**
Apeture Size	Select the Apeture Size. Note that above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support. ► Options: **128MB**, **256MB** (default)**, 512MB**, **1024MB** and **2048MB**
DVMT Pre-Allocated	Select the DVMT 5.0 Pre-allocated (Fixed) Graphic Memory size used by the Internal Graphic Device. ► Options: **32M** is the default.
DVMT Total Gfx Mem	Select the DVMT 5.0 Total Graphic Memory size used by the Internal Graphic Device. ► Options: **128MB, 256MB** (default) and **Max.**

3.3.4 PCI Express Configuration



Setting	Description
LAN 1~4	**Enable** (default) or **Disable** the PCI Express Root port.
M.2 E Key	
M.2 E key	**Enable** (default) or **Disable** the PCI Express root port.
ASPM Support	Set the ASPM Level: Force L0s - Force all links to L0s State: Auto - BIOS auto configure: DISABLE - Disable ASPM ► Options: **Disabled** (default), **L0s**, **L1**, **L0sL1** and **Auto**
PCIe Speed	Select PCI Express port speed. ► Options: **Auto**, **Gen1** (default), **Gen2** and **Gen3**

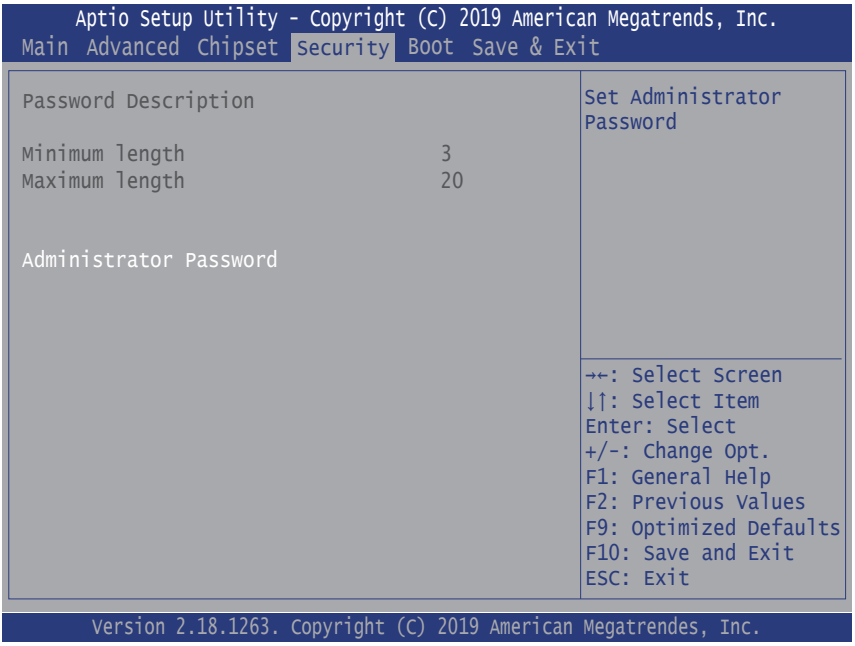
3.3.5 SATA And RST Configuration



Setting	Description
SATA Controller(s)	**Enable** (default) or **disable** SATA Device.
SATA Mode Selection	Determines how SATA controller(s) operate. ► Options: **AHCI** (default) and **RAID**
SATA Controller Speed	Indicates the maximum speed the SATA controller can support. ► Options: **Default** (default), **Gen1**, **Gen2**, **Gen3**
Port 0/1	**Enable** (default) or **disable** SATA Port.
SATA Device Type	Identify the SATA port is connected to **Solid State Drive** or **Hard Disk Drive** (default).

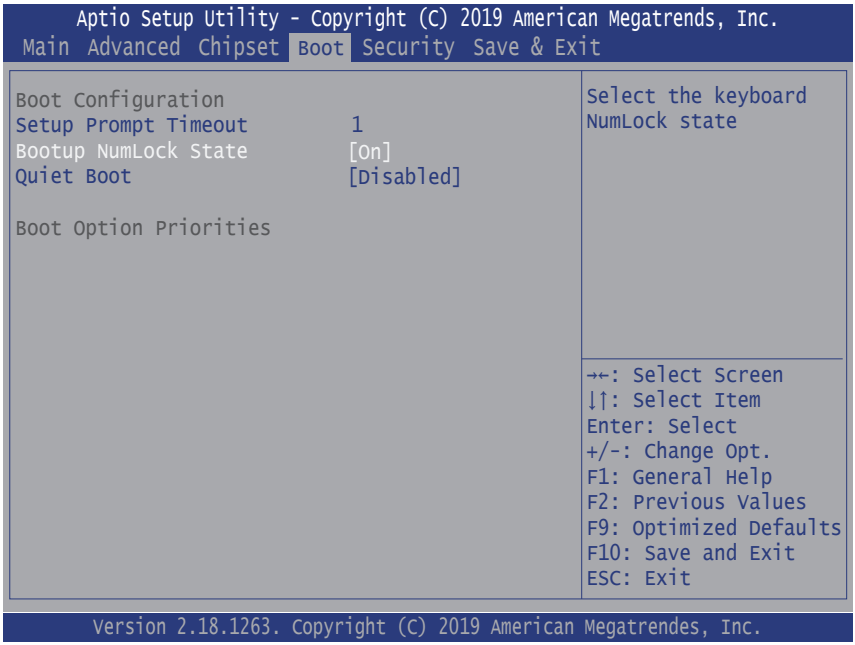
3.4 Security

The **Security** menu sets up the administrator password.



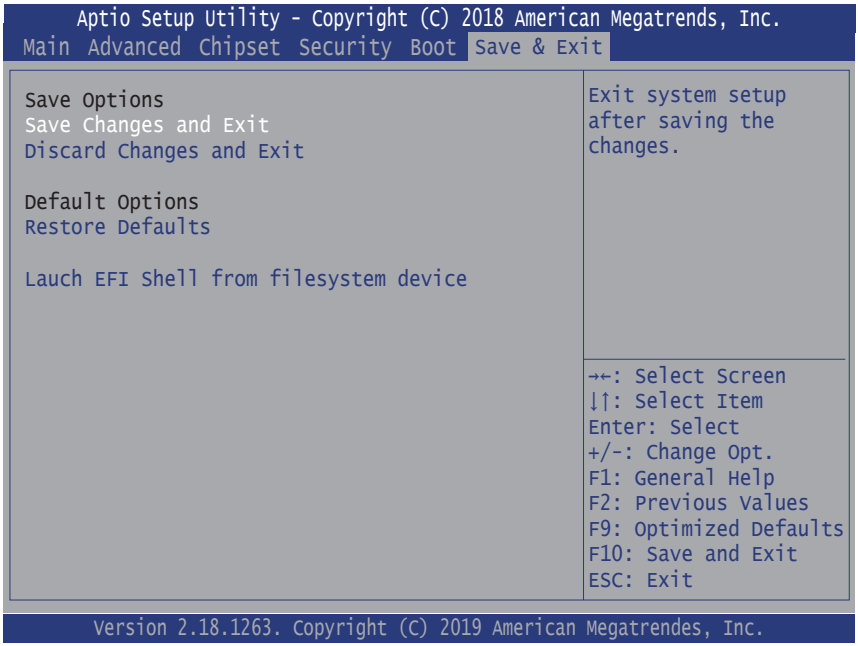
Setting	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. The screen then pops up an **Create New Password** dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

3.5 Boot



Setting	Description
Setup Prompt Timeout	Number of seconds to wati for setup activation key. 65535 (0XFFFF) means indefinite waiting.
Boot NumLock State	Select the keyboard NumLock state. ► Options: **On** (default) and **Off**.
Quiet Boot	**Enable** or **Disable** (default) Quiet Boot option.

3.6 Save & Exit



Setting	Description
Save Changes and Exit	Exit system setup after saving the changes. ► Enter the item and then a dialog box pops up: **Save configuration and exit? (Yes/ No)**
Discard Changes and Exit	Exit system setup without saving the changes. ► Enter the item and then a dialog box pops up: **Quit without saving? (Yes/ No)**
Restore Defaults	Restore/Load Default values for all the setup options. ► Enter the item and then a dialog box pops up: **Load Optimized Defaults? (Yes/ No)**
Launch EFI Shell from filesystem device	Attempts to launch EFI shell application (Shell.efi) from one of the available filesystem devices.

3.7 Beep Sound codes list

3.7.1 Boot Block Beep codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

3.7.2 POST BIOS Beep codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

3.7.3 Troubleshooting POST BIOS Beep codes

Number of Beeps	Description
1, 2 or 3	Reseat the memory, or replace known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem is solved.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

3.8 AMI BIOS Checkpoints

3.8.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS *(Note)*:

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done, including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module is not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enabled CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Perform main BIOS checksum and update recovery status accordingly.

D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and given control to it. Determine whether in memory.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leave all RAM below 1MB Read-Write, including E000 and F000 shadow areas, but close SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POS (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is waking from ACPI S3 state.
E1 - E8 EC - EE	OEM memory detection / configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from platform next to it.

3.8.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS *(Note)*:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L2 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration in line with the current configuration of the flash part.
FB	Set flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals to the recovery file size.
F4	The recovery file size does not equal to the found flash part size.

FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Set flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

3.8.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS *(Note)*:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also, initialize BIOS modules on POST entry and GPNV area. Initialize CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initialize data variables based on CMOS setup questions. Initialize both 8259 compatible PICs in the system.
05	Initialize the interrupt controlling hardware (generally, PIC) and interrupt vector table.
06	Do R/W test for CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Trap INT1Ch vector in "POSTINT1ChHandlerBlock."
07	Fix CPU POST interface calling pointer.
08	Initialize the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte after Auto detection of KB/MS uses AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor

C7	Early CPU Init Exit
0A	Initialize the 8042 compatible Key Board Controller.
0B	Detect the presence of PS/2 mouse.
0C	Detect the presence of Keyboard in KBC port.
0E	Test and initialize different input devices. Also, update the Kernel Variables. Trap the INT09h vector, so that the POST INT09h handler gets control over IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform of specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initialize different devices through DIM. See DIM Code Checkpoints section in document for more information.
2C	Initialize different devices. Detect and initialize the video adapter installed in the system that has optional ROMs.
2E	Initialize all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initialize the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any specific OEM information.
38	Initialize different devices through DIM. See DIM Code Checkpoints section in document for more information. USB controllers are initialized at this point.

39	Initialize DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, check for DEL keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…, etc.
52	Update CMOS memory size from memory found in memory test. Allocate memory for Extended BIOS Data Area from base memory. Program the memory hole or any kind of implementation that needs adjustment in system RAM size if needed.
60	Initialize NUM-LOCK status and program the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initialize IPL devices controlled by BIOS and optional ROMs.
7C	Generate and write contents for ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to user and get user's error response.
87	Execute BIOS setup if needed/requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disalbe NMI as selected.
90	Initialization of system management interrupted by invoking all handlers.
A1	Line-up work needed before booting to OS.
A2	Take care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initialize the Microsoft IRQ Routing Table. Prepare the runtime language module. Disable the system configuration display if needed.

A4	Initialize runtime language module. Display boot option's pop-up menu.
A7	Display the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initialize the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot, including final MTRR values.
00	Pass control to OS Loader (typically INT19h).

3.8.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST tries to initialize different system buses. The following table describes the main checkpoints where the DIM module is accessed *(Note)*:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and non-compliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set as automatic configuration and configures all remaining PnP and PCI devices.

While controlling in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble “X” indicates the function number that is being executed. “X” can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

3.8.5 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events *(Note)*:

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Enter sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Wake from sleep state S1, S2, S3, S4, or S5.

Note:
Please note that checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or optional ROMs from add-in PCI devices.

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Appendix

Appendix A. Watchdog Timer (WDT) Setting

WDT is widely used for industrial application to monitor CPU activities. The application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT timeout, the functional normal system will reload the WDT. The WDT never time-out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time-out and auto-reset the system to avoid abnormal operation.

This computer supports 255 levels watchdog timer by software programming I/O ports.

Below is an program example to disable and load WDT.

Sample Codes:

```
/*---------------------------------------------------------------------------*/
#include <math.h>
#include <stdio.h>
#include <dos.h>

int WDTCount;

int main(void)
{
          unsigned char       iCount;

          printf("WDT Times ( 1 ~ 255 ) : ");
          scanf("%d",&iCount);
          printf("\n");

          WDT_Start(iCount);

          return 0;
}

void WDT_Start(int iCount)
{
          outportb(0x66,0xBA);                    /* Enable Watch Dog */
          delay(1000);

          WDTCount = iCount;
          outportb(0x62, WDTCount);               /* Number is Watch Dog Down count number */
          delay(1000);

          outportb(0x62, 0x00);                   /* Minute is 1 count unit by minute */
                                                  /* Minute is 0 count unit by second */
}

void WDT_Stop(void)
{
          outportb(0x66,0xBB);                    /* Disable Watch Dog */
}

void WDT_Clear(void)
{
          outportb(0x66,0xBA);                    /* Enable Watch Dog */
          delay(1000);

          outportb(0x62, WDTCount);               /* Number is Watch Dog Down count number */
          delay(1000);
```

```
        outportb(0x62, 0x00);                    /* Minute is 1 count unit by minute
*/
                                                                              /  *
Minute is 0 count unit by second */
}
```

Appendix B. Digital I/O Setting

Digital I/O can read from or write to a line or an entire digital port, which is a collection of lines. This mechanism helps users achieve various applications such as industrial automation, customized circuit, and laboratory testing. Take the source code below that is written in C for the digital I/O application example.

Sample Codes:

```
/*-----   Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define    sioIndex  0x2E
#define    sioData   0x2F

/*-----   routing, sub-routing -----*/
void main()
{
    int iData;

    SioGPIOMode(0x0F);
    delay(2000);

    SioGPIOData(0x05);
    delay(2000);

    iData = SioGPIOStatus();
    printf(" Input : %2x \n",iData);
    delay(2000);

    SioGPIOData(0x0A);
    delay(2000);

    iData = SioGPIOStatus();
    printf(" Input : %2x \n",iData);
    delay(2000);
}

void SioGPIOMode(int iMode)
{
    outportb(sioIndex,0x87);                          /* Enable Super I/O */
    outportb(sioIndex,0x87);

    outportb(sioIndex,0x07);                          /* Select logic device - GPIO */
    outportb(sioData, 0x06);

    outportb(sioIndex,0x30);                          /* Enable GPIO */
    outportb(sioData, 0x01);

    outportb(sioIndex,0x88);                          /* GPIO 80~87 - Output Enable */
    outportb(sioData,iMode);

    outportb(sioIndex,0xAA);                          /* Disable Super I/O */
}

void SioGPIOData(int iData)
{
    outportb(sioIndex,0x87);                          /* Enable Super I/O */
```

```
    outportb(sioIndex,0x87);

    outportb(sioIndex,0x07);                        /* Select logic device - GPIO */
    outportb(sioData, 0x06);

    outportb(sioIndex,0x89);                        /* GPIO 80~87 - Output Data */
    outportb(sioData,iData);

    outportb(sioIndex,0xAA);                        /* Disable Super I/O */
}

int SioGPIOStatus()
{
    int iStatus = 0x00;

    outportb(sioIndex,0x87);                        /* Enable Super I/O */
    outportb(sioIndex,0x87);

    outportb(sioIndex,0x07);                        /* Select logic device - GPIO */
    outportb(sioData, 0x06);


    outportb(sioIndex,0x8A);                        /* GPIO 80~87 - Status */
    iStatus  = inportb(sioData);

    outportb(sioIndex,0xAA);                        /* Disable Super I/O */

    return iStatus;
}
```