EmETXe-i88U4

COM Express® Compact Type 6 CPU Module

User's Manual

Version 1.0

2020.07

Revision History

Version	Date	Description
1.0	2020.07	Initial release

Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class B

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please consult the user's manual first at:

http://www.arbor-technology.com

Please do not hesitate to call or e-mail our customer service when you still cannot find out the answer.

http://www.arbor-technology.com
E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1 The Product

The EmETXe-i88U4 is a space-conscious CPU board of 95 mm x 95 mm to take up only small footprint in your system. By the architecture of Type 6, the board has two high-performance connectors to promise stable data passing rate.

For system configuration, the board is supported by AMI UEFI BIOS. EmETXe-i88U4 is an ideal choice for some demanding industrial control and data communications by its significant processing performance, low power consumption and these features:

- Soldered onboard Intel® Xeon D-1539/D1508/D-1527 processor
- Supports two ECC SO-DIMM Sockets
- PCIex16 for Graphics
- Supports one Ethernet
- Operating Temp.: 0 ~ 60°C

1.2 About This Manual

This user's manual provides general information and installation instructions about the product. This user's manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. Please consult your vendor before further handling.

1.3 Specifications

System	
CPU	Soldered onboard Intel® Xeon D-1539 1.6GHz/D-1508 2.2GHz/D-1527 2.2GHzprocessor
Memory	2 x DDR4 ECC SO-DIMM sockets
BIOS	AMI UEFI BIOS
Watchdog Timer	1~255 levels reset
I/O	
USB 2.0	8 x USB 2.0 ports
USB 3.0	4 x USB 3.0 ports
Expansion Bus	1 x PCIex16 lane, 8 x PCIex1 lanes, I2C Interface
Digital I/O	8-bit Digital Input/Output
Storage	4 x Serial ATA ports with 600MB/s HDD transfer rate
Ethernet Chipset	1 x Intel® i210IT PCIe controller
TPM Function	Supports TPM (OEM request)
Mechanical & Environmental	
Power Requirement	+12V, 5VSB
Power Consumption	2.38A@12V (D1539 typical)
Operating Temp.	0 ~ 60°C (52 ~ 140°F)
Operating Humidity	10 ~ 95% @ 60ºC (non-condensing)
Dimension (L x W)	95 x 95 mm (3.7” x 3.7”)

1.4 Inside the Package

Before you begin installing your single board, please make sure that the following materials have been shipped:

1 x EmETXe-i88U4 COM Express CPU Module

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

1.5 Ordering Information

EmETXe-i88U4-D1539	Intel® Xeon D1539 COM Express® Compact Type 6 CPU module
EmETXe-i88U4-D1508	Intel® Xeon D1508 COM Express® Compact Type 6 CPU module
EmETXe-i88U4-D1527	Intel® Xeon D1527 COM Express® Compact Type 6 CPU module

1.5.1 Optional Accessories

HS-88U4-C1	Heat sink with FAN 95x95x36.5mm
PBE-1705-F1	COM Express® Type 6 evaluation carrier board with SIO F71869ED module in ATX form factor
CBK-03-1705-00	Cable kit • 1 x SATA cable • 2 x COM Flat cables

Driver (7.0A) Installation

To install the drivers,please contact your Arbor Sales Representative to get the permission to visit our website at **www.arbor.technology.com** and download the driver pack from the product page.

Driver	Path
SERVER	\EmETXe-i88U4\SERVER INF
RST	\EmETXe-i88U4\RST\GUI
Ethernet	\EmETXe-i88U4\Ethernet

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Chapter 2

Board Overview

2.1 What Is "COM Express®"?

With more and more demands on small and embedded industrial boards, a multi-functional COM (Computer-on-Module) surfaces as a great solution.

COM Express® supports seven pin-out types applying to Basic and Extended form factors:

Module Type 1 and 10 support single connector with two rows (220 pins).

Module Type 2, 3, 4, 5 and 6 support two connectors with four rows (440 pins).

EmETXe-i88U4 is a Type-6 module.

Difference between Standard Type 6 and EmETXe-i88U4 is listed as below:

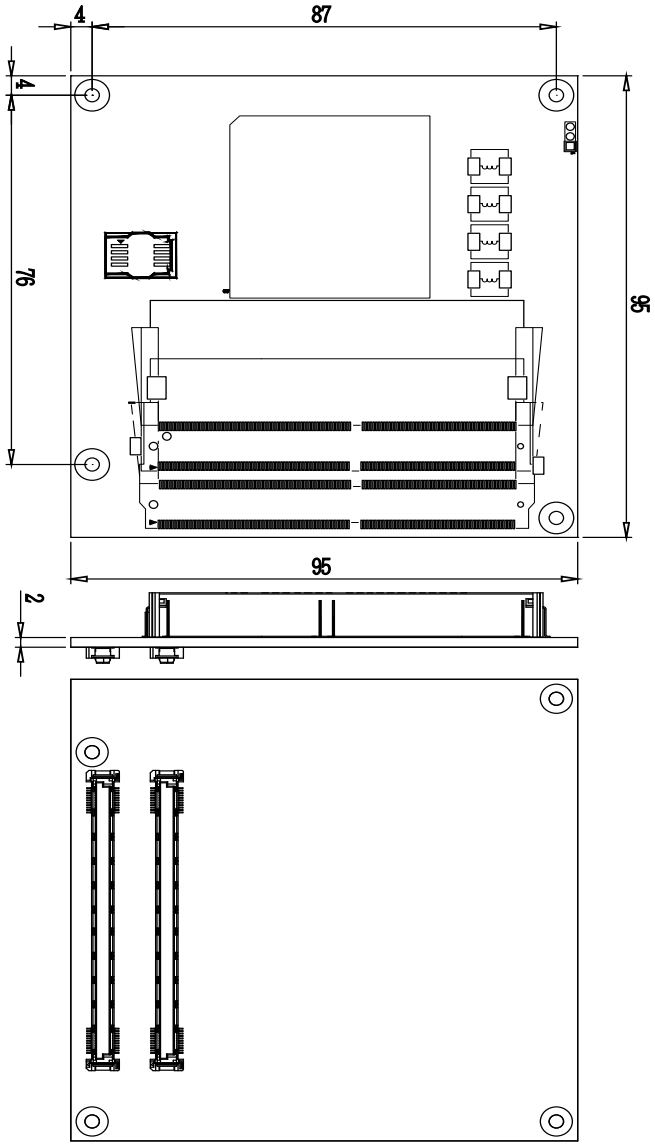
Module Type	Standard Type 6	EmETXe-i88U4
Connectors	2	2
Connector Rows	A, B, C, D	A, B, C, D
PCIe Lanes (Max)	24	24
LAN (Max)	1	1
Serial Ports (Max)	2	2
Digital Display I/F (Max)	3	0
USB 3.0 Ports (Max)	4	4

Row AB provides pins for PCI Express, SATA, LPC bus, system and power management, VGA, LAN, and power and ground interfaces.

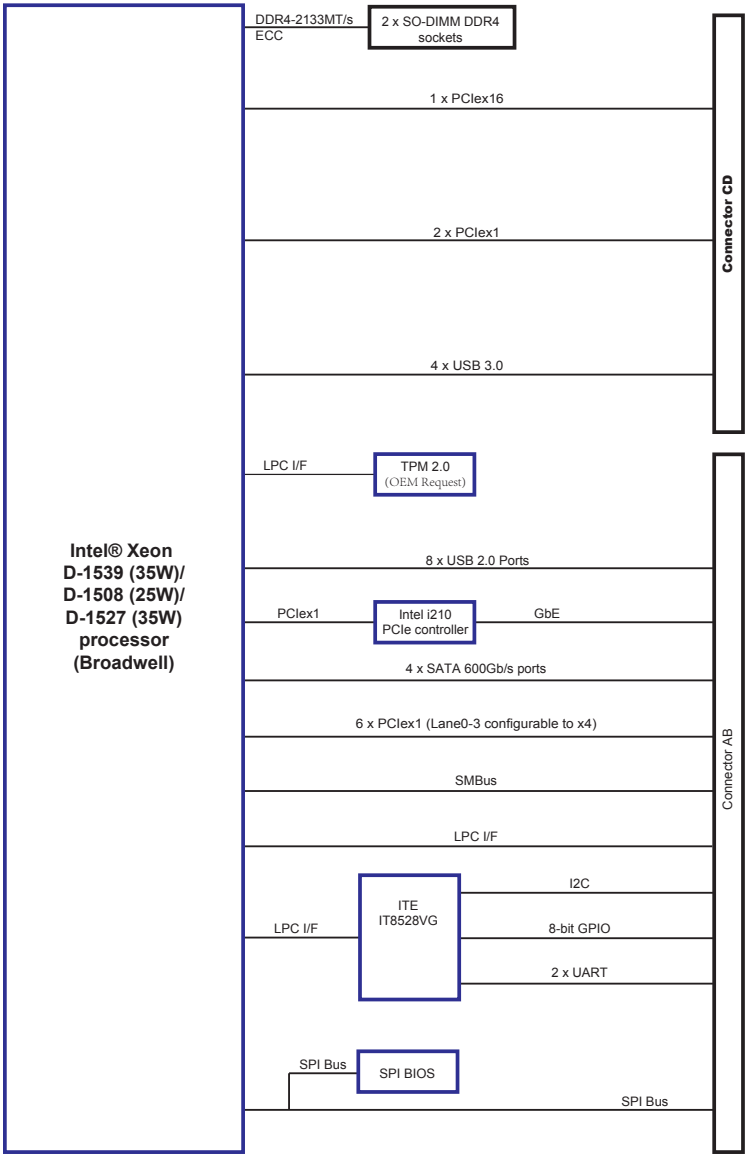
Row CD provides PCI Express, LAN and power and ground signals. The COM are targeted at following applications:

- Retail & Advertising
- Medical
- Test & Measurement
- Gaming & Entertainment
- Industrial & Automation
- Military & Government
- Security

2.2 Board Dimensions



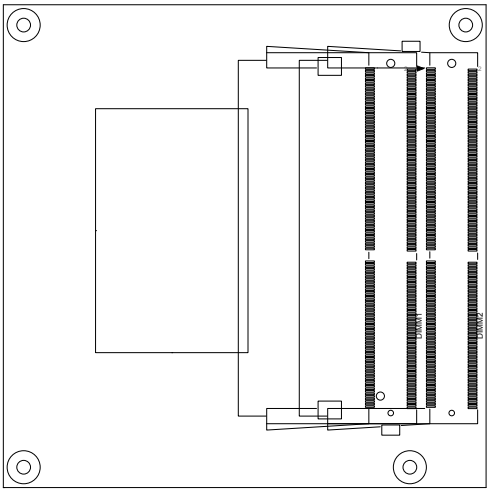
2.3 Block Diagram



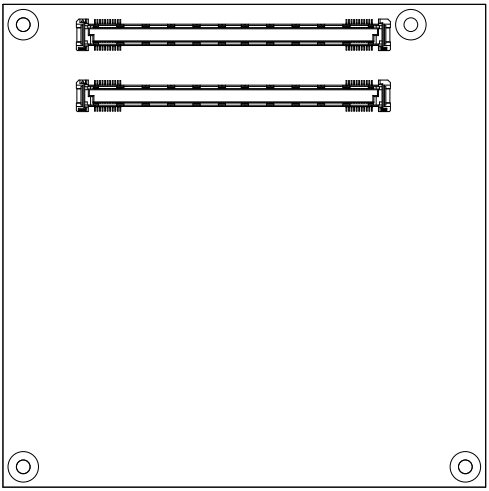
2.4 Connector Pin Definition

Being a most commonly-used Type 6, the EmETXe-i88U4 features two board-to-board connectors on bottom side.

Top Side



Bottom Side



COM Express AB Connector (bottom side)

B1	GND	GND	A1
B2	LAN_LED_LNK#_ACT	LAN1_MDI3N	A2
B3	LPC_FRAME#	LAN1_MDI3P	A3
B4	LPC_AD0	LAN_LED_100#	A4
B5	LPC_AD1	LAN_LED_1000#	A5
B6	LPC_AD2	LAN1_MDI2N	A6
B7	LPC_AD3	LAN1_MDI2P	A7
B8	+V3.3S	LAN_LED_LNK#	A8
B9	+V3.3S	LAN1_MDI1N	A9
B10	CLK_LPC_EXPRESS	LAN1_MDI1P	A10
B11	GND	GND	A11
B12	CB_PWRBTN#	LAN1_MDI0N	A12
B13	CB_SMB_CLK	LAN1_MDI0P	A13
B14	CB_SMB_DATA	N/C	A14
B15	CB_SMB_ALERT#	SLP_S3#	A15
B16	SATA_TXP1_C	SATA_TXP0_C	A16
B17	SATA_TXN1_C	SATA_TXN0_C	A17
B18	SUS_STAT#	SLP_S4#	A18
B19	SATA_RXP1_C	SATA_RXP0_C	A19
B20	SATA_RXN1_C	SATA_RXN0_C	A20
B21	GND	GND	A21
B22	SATA_TXP3_C	SATA_TXP2_C	A22
B23	SATA_TXN3_C	SATA_TXN2_C	A23
B24	CB_PWROK	SLP_S5#	A24
B25	SATA_RXP3_C	SATA_RXP2_C	A25
B26	SATA_RXN3_C	SATA_RXN2_C	A26
B27	WDT	BATLOW#	A27
B28	N/C	SATALED#	A28
B29	N/C	N/C	A29
B30	N/C	N/C	A30
B31	GND	GND	A31
B32	SPKR	N/C	A32
B33	I2C_CLK	N/C	A33
B34	I2C_DAT	BIOS_DIS0#	A34
B35	THRM#	THRMTRIP#	A35
B36	USBDN5_DN	USBDN4_DN	A36
B37	USBDN5_DP	USBDN4_DP	A37
B38	USB_OC2_N	USB_OC3_N	A38
B39	USBDN3_DN	USBDN2_DN	A39
B40	USBDN3_DP	USBDN2_DP	A40
B41	GND	GND	A41
B42	USBDN1_DN	USB_2N	A42
B43	USBDN1_DP	USB_2P	A43
B44	USB_OC0_N	USB_OC1_N	A44
B45	USB_1N	USB_0N	A45
B46	USB_1P	USB_0P	A46
B47	PLTRST#_BUFF	VCC_RTC	A47
B48	EXCD1_CCPE#	PLTRST#_BUFF	A48
B49	CB_SYSRST#	EXCD0_CPPE#	A49
B50	CB_RESET#	SERIRQ	A50
B51	GND	GND	A51
B52	PCIE_RXP6	PCIE_TXP6	A52
B53	PCIE_RXN6	PCIE_TXN6	A53
B54	DIO_5	DIO_0	A54
B55	PCIE_RXP5	PCIE_TXP5	A55

B56	PCIE_RXN5	PCIE_TXN5	A56
B57	DIO_6	GND	A57
B58	PCIE_RXP4	PCIE_TXP4	A58
B59	PCIE_RXN4	PCIE_TXN4	A59
B60	GND	GND	A60
B61	PCIE_RXP3	PCIE_TXP3	A61
B62	PCIE_RXN3	PCIE_TXN3	A62
B63	DIO_7	DIO_1	A63
B64	PCIE_RXP2	PCIE_TXP2	A64
B65	PCIE_RXN2	PCIE_TXN2	A65
B66	PCH_WAKE#	GND	A66
B67	EC_WAKE_IN#	DIO_2	A67
B68	PCIE_RXP1	PCIE_TXP1	A68
B69	PCIE_RXN1	PCIE_TXN1	A69
B70	GND	GND	A70
B71	N/C	N/C	A71
B72	N/C	N/C	A72
B73	N/C	N/C	A73
B74	N/C	N/C	A74
B75	N/C	N/C	A75
B76	N/C	N/C	A76
B77	N/C	N/C	A77
B78	N/C	N/C	A78
B79	N/C	N/C	A79
B80	GND	GND	A80
B81	N/C	N/C	A81
B82	N/C	N/C	A82
B83	N/C	N/C	A83
B84	VCC_5V_SBY	N/C	A84
B85	VCC_5V_SBY	DIO_3	A85
B86	VCC_5V_SBY	N/C	A86
B87	VCC_5V_SBY	N/C	A87
B88	BIOS_DIS1#	COM_EXP_CLK_P	A88
B89	N/C	COM_EXP_CLK_N	A89
B90	GND	GND	A90
B91	N/C	SPI_POWER	A91
B92	N/C	SPI_MISO	A92
B93	N/C	DIO_4	A93
B94	N/C	SPI_CLK	A94
B95	N/C	SPI_MOSI	A95
B96	N/C	COM_TPM_PP	A96
B97	SPI_CS0#	N/C	A97
B98	N/C	UART_TX0	A98
B99	N/C	UART_RX0	A99
B100	GND	GND	A100
B101	FAN_PWMOUT	UART_TX1	A101
B102	FAN_TACHIN	UART_RX1	A102
B103	SLEEP#	LID#	A103
B104	VCC_12V	VCC_12V	A104
B105	VCC_12V	VCC_12V	A105
B106	VCC_12V	VCC_12V	A106
B107	VCC_12V	VCC_12V	A107
B108	VCC_12V	VCC_12V	A108
B109	VCC_12V	VCC_12V	A109
B110	GND	GND	A110

COM Express CD Connector (bottom side)

D1	GND	GND	C1
D2	GND	GND	C2
D3	USB3_TXN1	USB3_RXN1	C3
D4	USB3_TXP1	USB3_RXP1	C4
D5	GND	GND	C5
D6	USB3_TXN2	USB3_RXN2	C6
D7	USB3_TXP2	USB3_RXP2	C7
D8	GND	GND	C8
D9	USB3_TXN5	USB3_RXN5	C9
D10	USB3_TXP5	USB3_RXP5	C10
D11	GND	GND	C11
D12	USB3_TXN6	USB3_RXN6	C12
D13	USB3_TXP6	USB3_RXP6	C13
D14	GND	GND	C14
D15	N/C	N/C	C15
D16	N/C	N/C	C16
D17	N/C	N/C	C17
D18	N/C	N/C	C18
D19	PCIE_TXP7	PCIE_RXP7	C19
D20	PCIE_TXN7	PCIE_RXN7	C20
D21	GND	GND	C21
D22	PCIE_TXP8	PCIE_RXP8	C22
D23	PCIE_TXN8	PCIE_RXN8	C23
D24	N/C	N/C	C24
D25	N/C	N/C	C25
D26	N/C	N/C	C26
D27	N/C	N/C	C27
D28	N/C	N/C	C28
D29	N/C	N/C	C29
D30	N/C	N/C	C30
D31	GND	GND	C31
D32	N/C	N/C	C32
D33	N/C	N/C	C33
D34	N/C	N/C	C34
D35	N/C	N/C	C35
D36	N/C	N/C	C36
D37	N/C	N/C	C37
D38	N/C	N/C	C38
D39	N/C	N/C	C39
D40	N/C	N/C	C40
D41	GND	GND	C41
D42	N/C	N/C	C42
D43	N/C	N/C	C43
D44	N/C	N/C	C44
D45	N/C	N/C	C45
D46	N/C	N/C	C46
D47	N/C	N/C	C47
D48	N/C	N/C	C48
D49	N/C	N/C	C49
D50	N/C	N/C	C50
D51	GND	GND	C51
D52	PE1_TX_DP_0	PE1_RX_DP_0	C52
D53	PE1_TX_DN_0	PE1_RX_DN_0	C53
D54	+V3.3S	N/C	C54
D55	PE1_TX_DP_1	PE1_RX_DP_1	C55

D56	PE1_TX_DN_1	PE1_RX_DN_1	C56
D57	TYPE2#	N/C	C57
D58	PE1_TX_DP_2	PE1_RX_DP_2	C58
D59	PE1_TX_DN_2	PE1_RX_DN_2	C59
D60	GND	GND	C60
D61	PE1_TX_DP_3	PE1_RX_DP_3	C61
D62	PE1_TX_DN_3	PE1_RX_DN_3	C62
D63	N/C	N/C	C63
D64	N/C	N/C	C64
D65	PE1_TX_DP_4	PE1_RX_DP_4	C65
D66	PE1_TX_DN_4	PE1_RX_DN_4	C66
D67	N/C	N/C	C67
D68	PE1_TX_DP_5	PE1_RX_DP_5	C68
D69	PE1_TX_DN_5	PE1_RX_DN_5	C69
D70	GND	GND	C70
D71	PE1_TX_DP_6	PE1_RX_DP_6	C71
D72	PE1_TX_DN_6	PE1_RX_DN_6	C72
D73	GND	GND	C73
D74	PE1_TX_DP_7	PE1_RX_DP_7	C74
D75	PE1_TX_DN_7	PE1_RX_DN_7	C75
D76	GND	GND	C76
D77	N/C	N/C	C77
D78	PE1_TX_DP_8	PE1_RX_DP_8	C78
D79	PE1_TX_DN_8	PE1_RX_DN_8	C79
D80	GND	GND	C80
D81	PE1_TX_DP_9	PE1_RX_DP_9	C81
D82	PE1_TX_DN_9	PE1_RX_DN_9	C82
D83	N/C	N/C	C83
D84	GND	GND	C84
D85	PE1_TX_DP_10	PE1_RX_DP_10	C85
D86	PE1_TX_DN_10	PE1_RX_DN_10	C86
D87	GND	GND	C87
D88	PE1_TX_DP_11	PE1_RX_DP_11	C88
D89	PE1_TX_DN_11	PE1_RX_DN_11	C89
D90	GND	GND	C90
D91	PE1_TX_DP_12	PE1_RX_DP_12	C91
D92	PE1_TX_DN_12	PE1_RX_DN_12	C92
D93	GND	GND	C93
D94	PE1_TX_DP_13	PE1_RX_DP_13	C94
D95	PE1_TX_DN_13	PE1_RX_DN_13	C95
D96	GND	GND	C96
D97	N/C	N/C	C97
D98	PE1_TX_DP_14	PE1_RX_DP_14	C98
D99	PE1_TX_DN_14	PE1_RX_DN_14	C99
D100	GND	GND	C100
D101	PE1_TX_DP_15	PE1_RX_DP_15	C101
D102	PE1_TX_DN_15	PE1_RX_DN_15	C102
D103	GND	GND	C103
D104	VCC_12V	VCC_12V	C104
D105	VCC_12V	VCC_12V	C105
D106	VCC_12V	VCC_12V	C106
D107	VCC_12V	VCC_12V	C107
D108	VCC_12V	VCC_12V	C108
D109	VCC_12V	VCC_12V	C109
D110	GND (FIXED)	GND	C110

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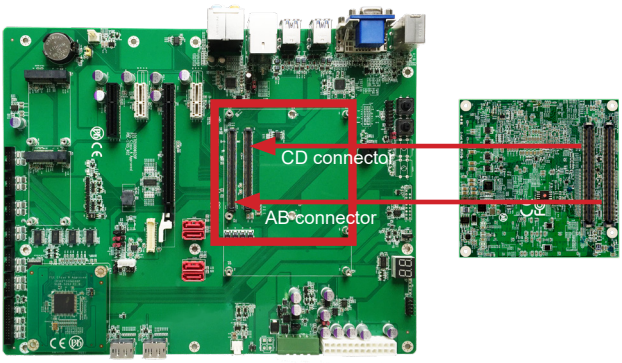
Chapter 3

Installation & Maintenance

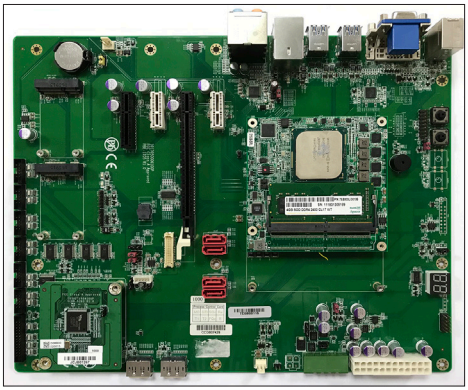
3.1 Installing the CPU Module to Carrier Board

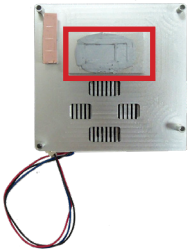
1. Mount the EmETXe-i88U4 into PBE-1705 via COM Express connectors as below; that is, COM Express AB to AB and CD to CD.



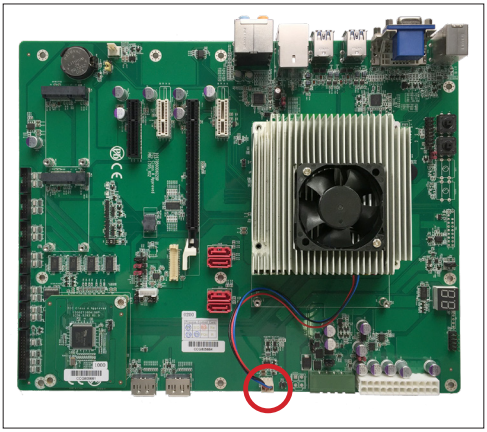
2. Install the optional heat spreader or heat sink with fan to the COM module.

   Apply thermal grease to the CPU area on the CPU module. Place the heat sink over the CPU module and fasten the six screws to secure it in place.





Then connect the fan cable to the fan connector on the carrier board.



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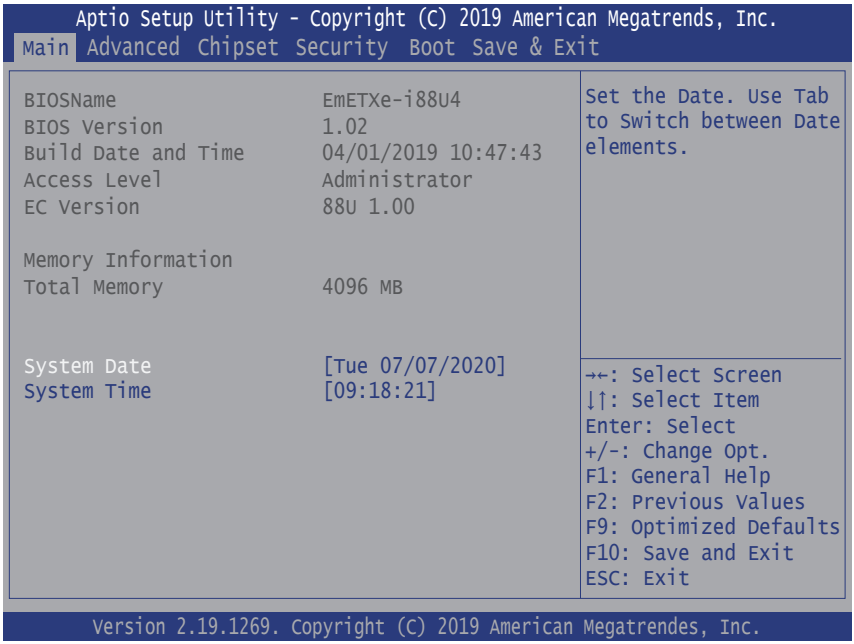
Chapter 4

BIOS

4.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **"Delete"** once the power is turned on.

The **Main Setup** screen lists the following information:



Setting	Description
System Language	Choose the system default language.
System Date	Set the system date. Use Tab to switch between Data elements. Note that the 'Day' automatically changes when you set the date. ► The date format is: **Day:** Sun to Sat **Month:** 1 to 12 **Date:** 1 to 31 **Year:** 1998 to 2099

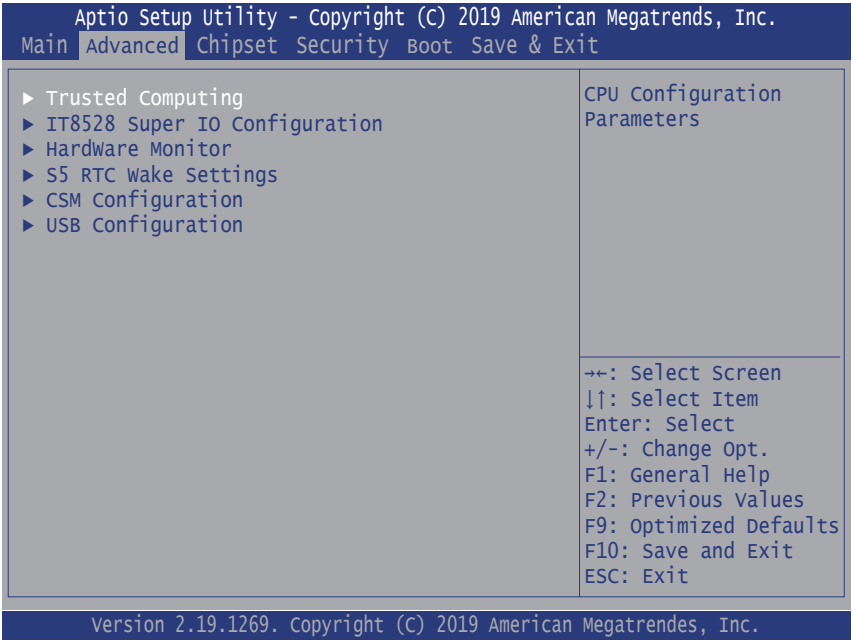
System Time	Set the system time. Use Tab to switch between Time elements. ► The time format is: **Hour:** 00 to 23 **Minute:** 00 to 59 **Second:** 00 to 59

Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

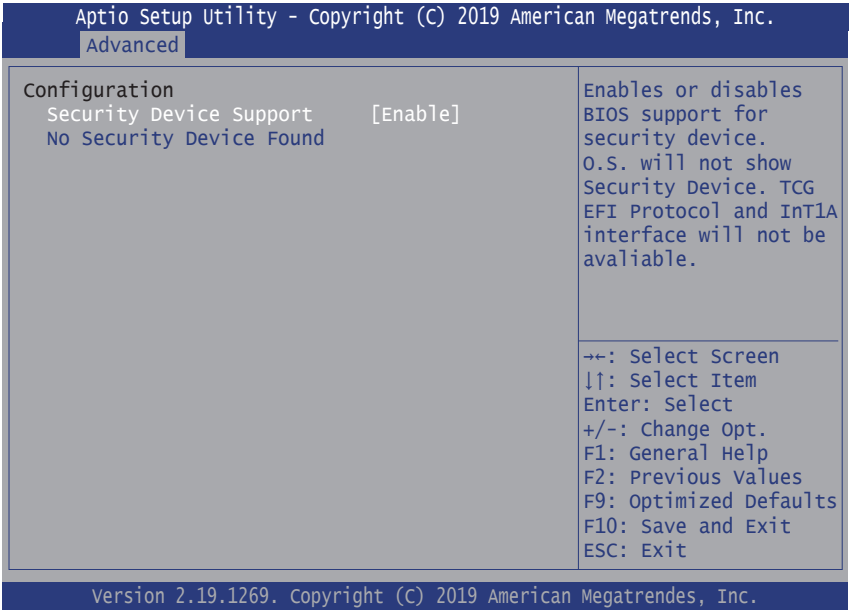
Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down / -	Decrease the numeric value on a selected setup item / make change
F1	Activate “General Help” screen
F2	Restore previous values
F9	Load optimized values
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm)

4.2 Advanced



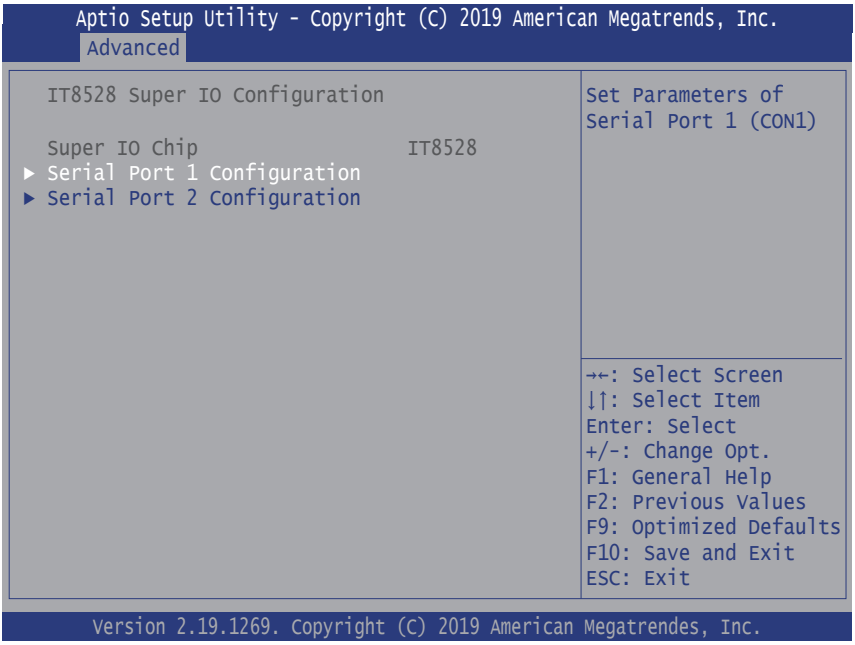
Setting	Description
Trusted Computing	See 4.2.1 Trusted Computing on page 23
IT8528 Super IO Configuration	See 4.2.2 IT8528 Super IO Configuration on page 24
Hardware Monitor	See 4.2.3 Hardware Monitor on page 25
S5 RTC Wake Settings	See 4.2.4 S5 RTC Configuration on page 26
CSM Configuration	See 4.2.5 CSM Configuration on page 27
USB Configuration	See 4.2.6 USB Configuration on page 29

4.2.1 Trusted Computing



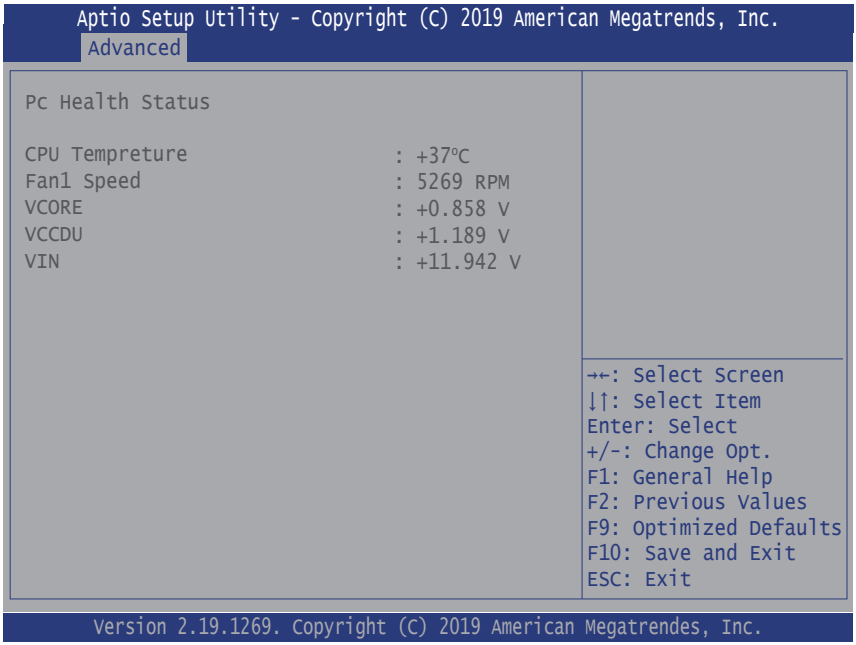
Setting	Description
Security Device Support	**Enable** (default) or **Disable** BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

4.2.2 IT8528 Super IO Configuration



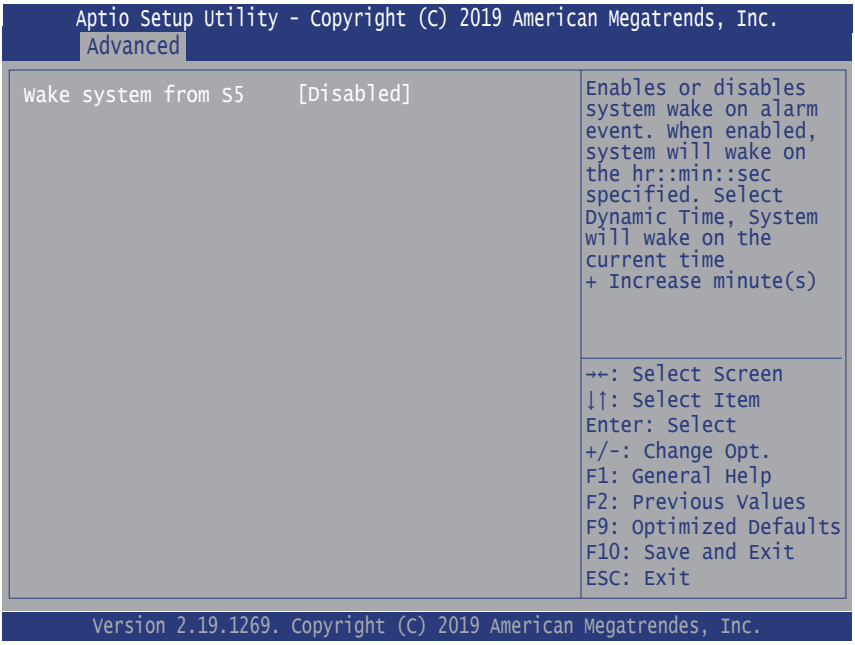
Setting	Description
Serial Port	**Enable** (default) or **Disable** serial port (COM).
Change Settings	Select an optimal setting for the super IO device. ▶ Serial Port 1 default: **IO=3F8h; IRQ=4;** ▶ Serial Port 2 default: **IO=2F8h; IRQ=3;**

4.2.3 Hardware Monitor



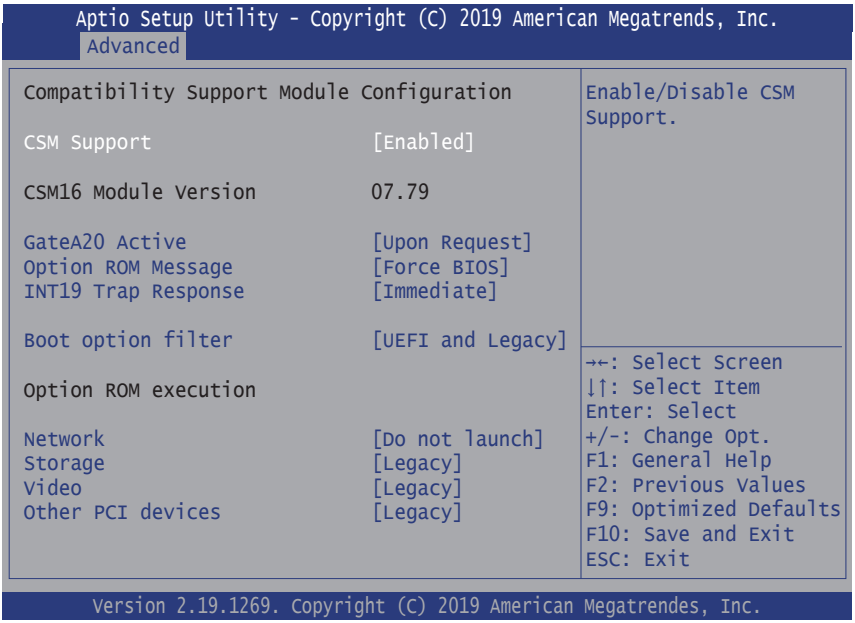
Access this submenu to monitor the hardware status.

4.2.4 S5 RTC Configuration



Setting	Description
Wake System from S5	**Enable** or **Disable** (default) system wake on alarm event. ► Options available are: **Disabled** (default): **Fixed Time:** System will wake on the hr::min::sec specifiedc. **DynamicTime:** If selected, you need to set **Wake up minute increase** from 1 - 5. System will wake on the current time + increase minute(s).

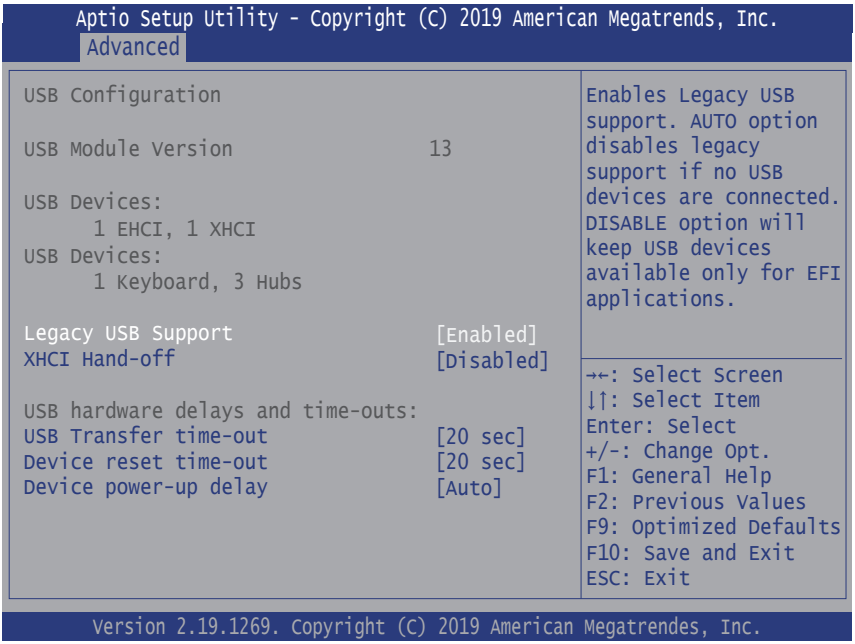
4.2.5 CSM Configuration



Setting	Description
CSM Support	**Enable** (default) or **Disable** CSM Support
GateA20 Active	Select setting for GateA20. Options include: ► **Upon Request** (default) - GA20 can be disabled using BIOS services. ► **Always** - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Message	Select display mode for Option ROM. ► Options: **Force BIOS** (default), and **Keep Current**.
INT19 Trap Response	BIOS reaction on INT19 trapping by Option ROM. Options include: ► **Immediate** (default) - Execute the trap right away ► **Postponed** - Execute the trap during legacy boot.
Boot option filter	Controls Legacy/UEFI ROMs priority. ► Options: **UEFI and Legacy** (default), **Legacy only** and **UEFI only**

Network	Control the execution of UEFI and Legacy PXE OpROM. ► Options: **Do not launch** (default), **UEFI** and **Legacy**
Storage	Control the execution of UEFI and Legacy Storage OpROM. ► Options: **Do not launch**, **UEFI** (default) and **Legacy**
Video	Control the execution of UEFI and Legacy Video OpROM. ► Options: **Do not launch**, **UEFI** and **Legacy** (default)
Other PCI device	Set the OpROM execution policy for devices other than Network, Storage, or Video. ► Options: **Do not launch**, **UEFI** and **Legacy** (default)

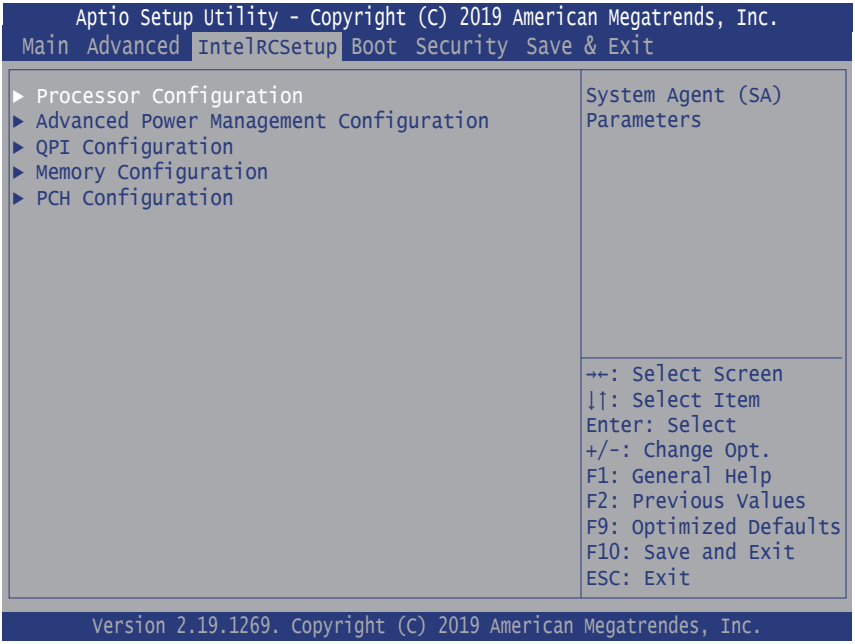
4.2.6 USB Configuration



Setting	Description
Legacy USB Support	Sets legacy USB support. ► Options: **Enabled** (default), **Disabled** and **Auto**. **AUTO** option disables legacy support if no USB devices are connected. **Disable** option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enable** (default) or **Disable** XHCI Hand-off This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB hardware delay and time-out	

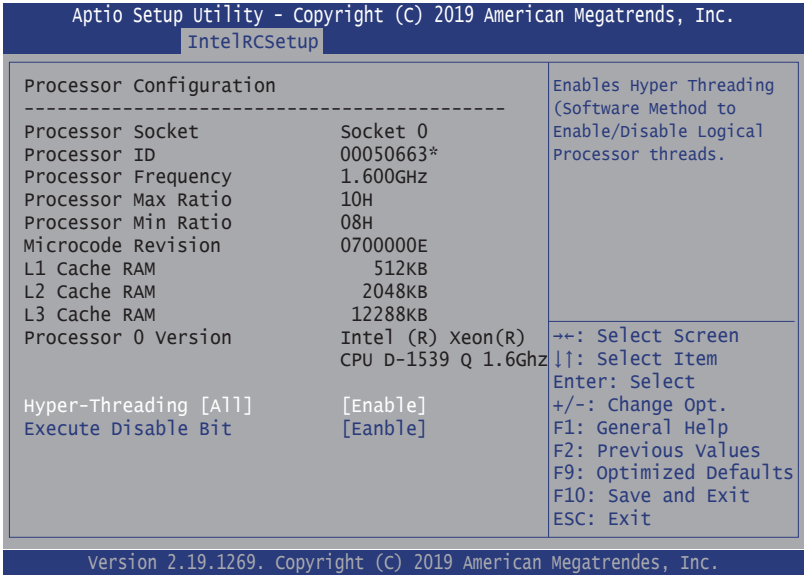
USB Transfer time-out	Use this item to set the time-out value for control, bulk, and interrupt transfers. ▶ Options available are: **1 sec, 5 sec, 10 sec, 20 sec** (default)
Device reset time-out	Use this item to set USB mass storage device start unit command time-out. ▶ Options available are: **10 sec, 20 sec** (default)**, 30 sec, 40 sec**
Device power-up delay	Use this item to set maximum time the device will take before it properly reports itself to the host controller. Options available are: ▶ **Auto** (Default): 'Auto' uses default value: for a root port it is 100 ms, for a hub port the delay is taken from hub descriptor. ▶ **Manual**: Select **Manual** you can set value for the following sub-item: '**Device Power-up delay in seconds**', the delay range in from 1 to 40 seconds, in one second increments.

4.3 IntelRCSetup



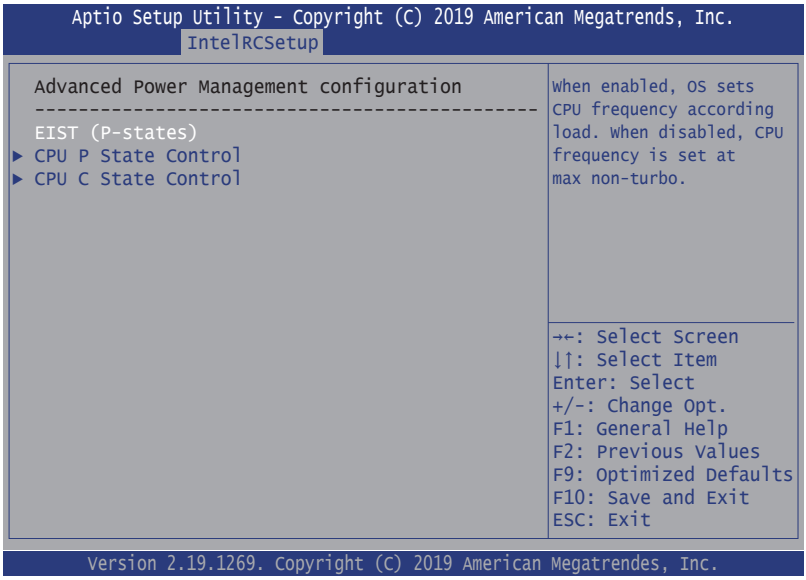
Setting	Description
Processor Configuration	See 4.3.1 Processor Configuration on page 32
Advanced Power Management Configuration	See 4.3.2 Advanced Power Management Configuration on page 33
QPI Configuration	See 4.3.3 QPI Configuration on page 36
Memory Configuration	See 4.3.4 Memory Configuration on page 40
PCH Configuration	See 4.3.5 PCH Configuration on page 41

4.3.1 Processor Configuration



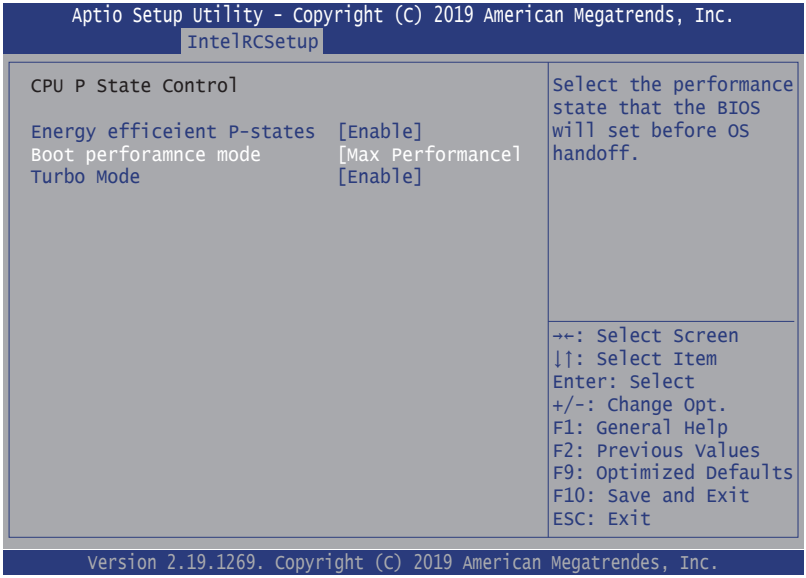
Setting	Description
Hyper-Threading	**Enable** (default) or **Disable** Hyper Threading (Software method to enable/disable logical processor threads.
Execute Disable Bit	When disabled, forces the XD feature flag to always return 0. Default: **Enabled**

4.3.2 Advanced Power Management Configuration



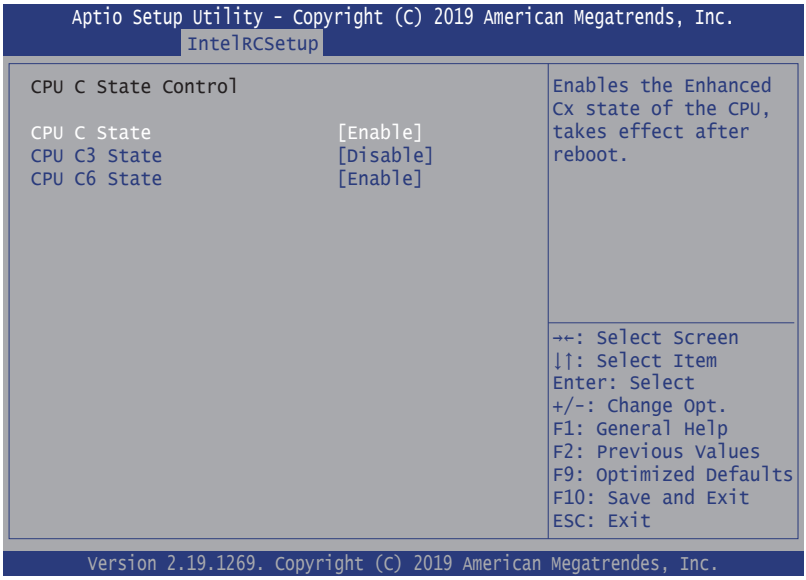
Setting	Description
EIST (P-states)	When enabled, OS sets CPU frequency according load. When disabled, CPU frequency is set at max non-turbo. Default: **Enabled**
CPU P State Control	See 4.3.2.1 CPU P State Control on page 34
CPU C State Control	See 4.3.2.2 CPU C State Control on page 35

4.3.2.1 CPU P State Control



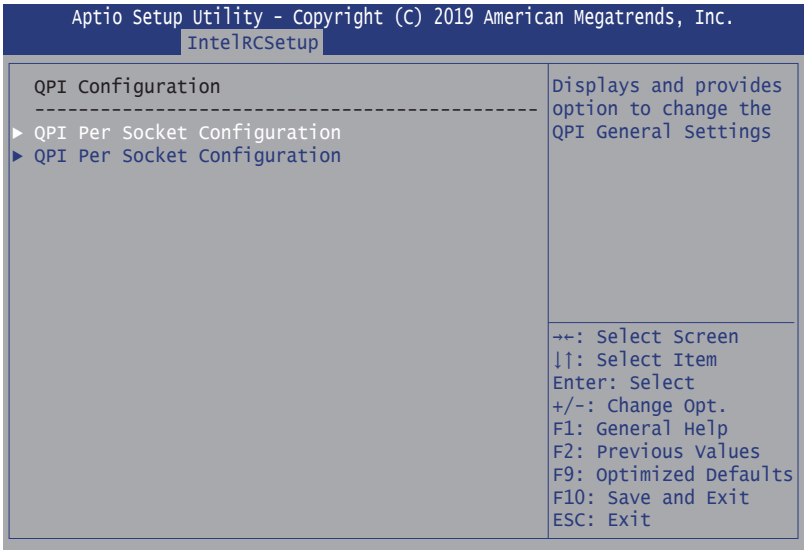
Setting	Description
Energy efficient P-states	**Enable** (default) or **Disable** Energy efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID function 6 EAX [3] will read 0 indicating no support for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_ PERFORMANCE_BIAS MSR.
Boot performance mode	Select the performance state that the BIOS will set before OS handoff. ► Options: **Max Performance** (default) and **Max Efficient**.
Turbo Mode	**Enable** (default) or **Disable** Turbo Mode. Turbo mode allows a CPU logical processor to execute a higher frequency when enough power is available not exceed CPU defined limits.

4.3.2.2 CPU C State Control



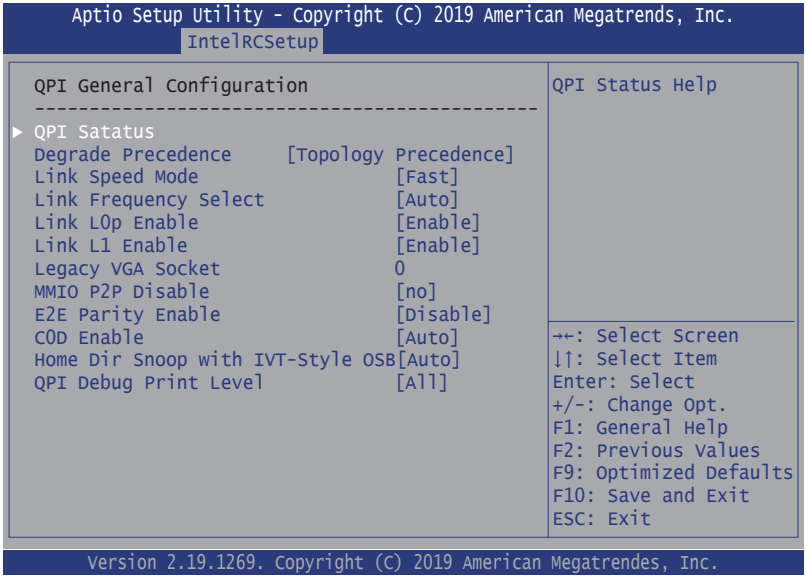
Setting	Description
CPU C State	**Enable** (default) or **Disable** the Enhanced Cx state of the CPU, takes effect after reboot.
CPU C3 State	**Enable** or **Disable** (default) the CPU C3 (ACPI C2 report to OS. Recommended to be disabled.
CPU C6 State	**Enable** (default) or **Disable** the CPU C6 (ACPI C2 report to OS. Recommended to be enabled.

4.3.3 QPI Configuration



Setting	Description
QPI General Configuration	See 4.3.3.1 QPI General Configuration on page 37
QPI Per Socket Configuration	See 4.3.3.2 QPI Per Socket Configuration on page 39

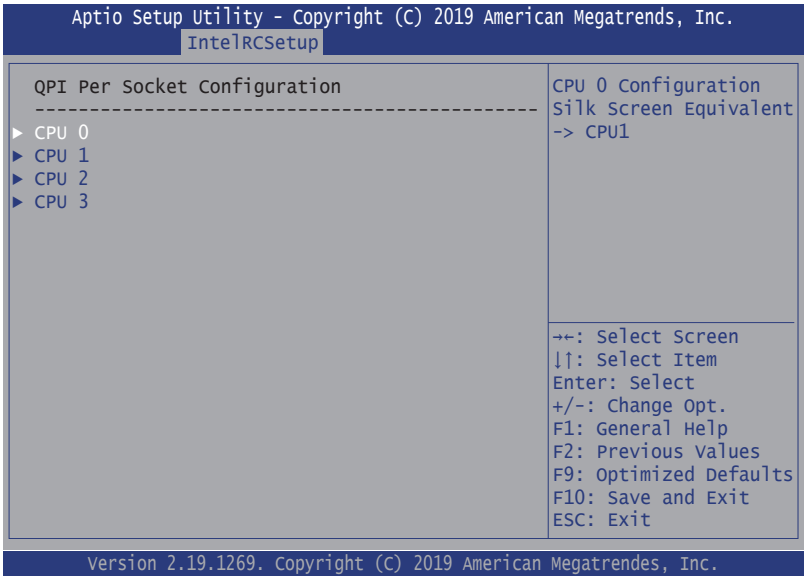
4.3.3.1 QPI General Configuration



Setting	Description
QPI Status	To view QPI status.
Degrade Precedence	Choose Topology Precedence to degrade features if system options are in conflict or choose Feature Precedence to degrade topology if system options are in conflict. ► Options: **Topology Precedence** (default) and **Feature Precedence**
Link Speed Mode	Select the QPI link speed as either the POR speed (Fast) or default speed (Slow). ► Options: **Fast** (default) and **Slow**
Link Frequency Select	Allows for selecting the QPI Link Frequency. ► Options: **6.4GB/s**, **8.0GB/s**, **9.6GB/s**, **Auto** (default) and **Auto Limited**
Link L0p Enable	**Enable** (default) or **Disable** Link L0p
Link L1 Enable	**Enable** (default) or **Disable** Link L1p

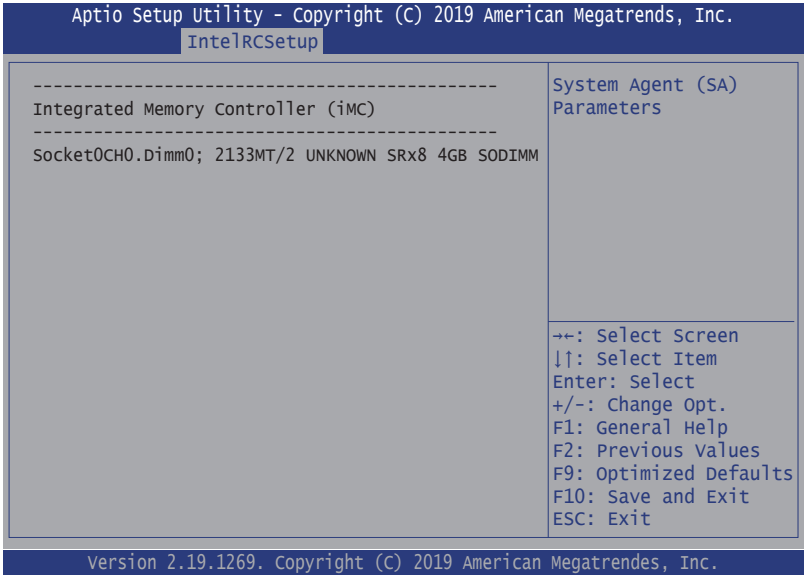
Legacy VGA Socket	Socket that claims the legacy VGA ranges; valid values are 0~7; **0** is the default.
MMIO P2P Disable	To disable MMIOL P2P traffic across sockets. Default is **No** to not disable.
E2E Parity Enable	**Enable** or **Disable** (default) E2E Parity.
COD Enable	**Enable** or **Disable** Cluster on Die. ► Options: **Disable**, **Enable** and **Auto** (default)
Early Snoop	**Enable** or **Disable** early snoop. ► Options: **Disable**, **Enable** and **Auto** (default)
Home Dir Snoop with IVT-Style OSB	**Enable** or **Disable** home DIR Snoop with IVT-Style OSB. ► Options: **Disable**, **Enable** and **Auto** (default)
QPI Debug Print Level	Configures QPI Debug Print Level. ► Options: **Fatal**, **Warning**, **Summary**, **Detail** and **All** (default)

4.3.3.2 QPI Per Socket Configuration



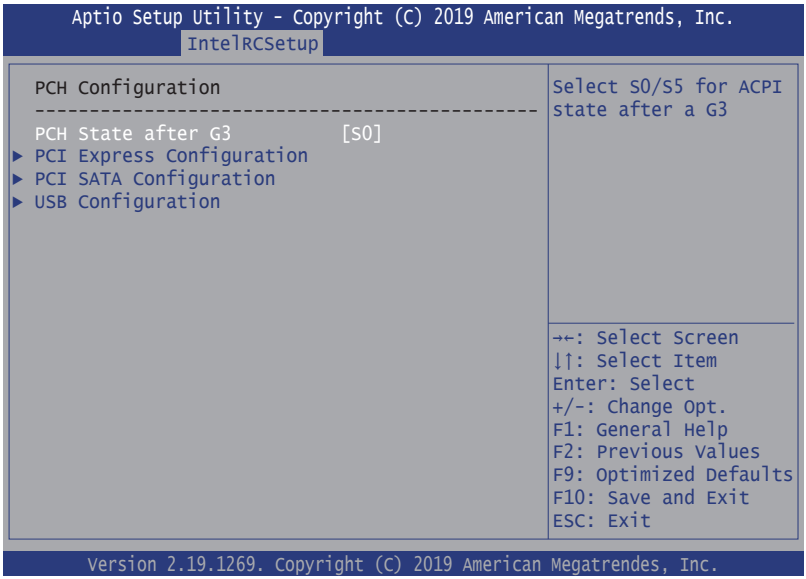
Setting	Description
Bus Resources Allocation Ratio	Configure bus resources allocation ratio, range 0 to 8.
IO Resources Allocation Ratio	Configure IO resources allocation ratio, range 0 to 8.
MMIOL Resources Allocation Ratio	Configure MMIOL resources allocation ratio, range 0 to 8.
IIO Disable	Configure disabling ports and clock gate IIO. ► Options: **No** (default) **Disable Ports and IIO without memory hotplug** **Disable Ports OIny with memory hotplug**

4.3.4 Memory Configuration



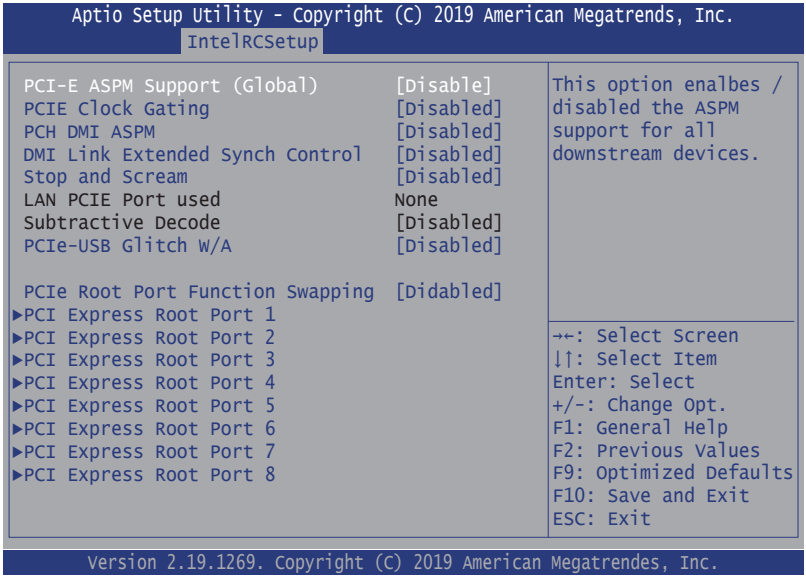
Access this submenu to monitor the memory configuration.

4.3.5 PCH Configuration



Setting	Description
PCH State after G3	Select S0/S5 for ACPI state after a G3. ► Options: **S0** (default) and **S5**
PCI Express Configuration	See 4.3.5.1 PCI Express Configuration on pa ge 42
PCI SATA Configuration	See 4.3.5.2 PCI SATA Configuration on page 44
USB Configuration	See 4.3.5.3 USB Configuration on page 45

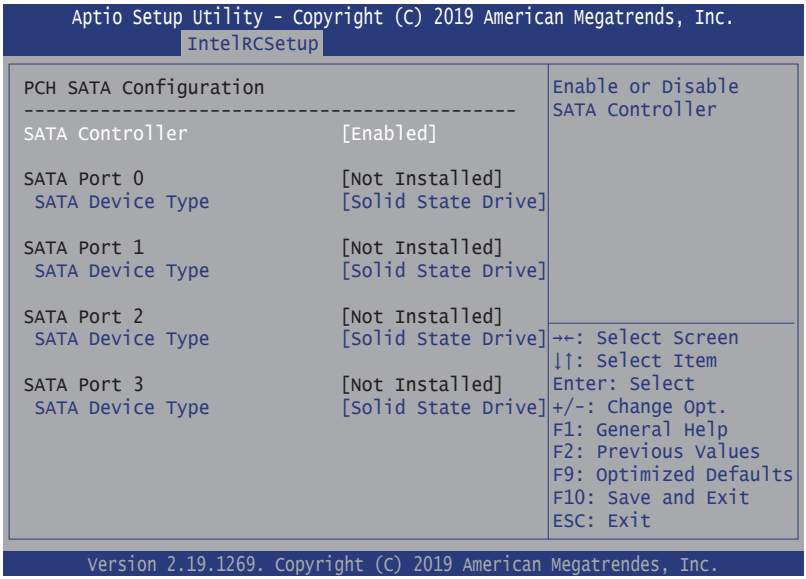
4.3.5.1 PCI Express Configuration



Setting	Description
PCI-E ASPM Support	This option enables / disables the ASPM support for all downstream devices. ▶ Options: **Disabled** (default) and **L1 only**
PCIE Clock Gating	**Enable** or **Disable** (default) PCIE Clock Gating for all PCH PCIE Ports.
PCH DMI ASPM	**Enable** or **Disable** (default) PCH DMI ASPM setting.
DMI Link Extended Synch Control	**Enable** or **Disable** (default) the control of Extended Synch on SB side of the DMI Link.
Stop and Scream	When enabled DS packets on DMI with the EP bit set, wil have their UT bit set.
LAN PCIE Port used	Show LAN PCIE Port used.
Subtractive Decode	N/A

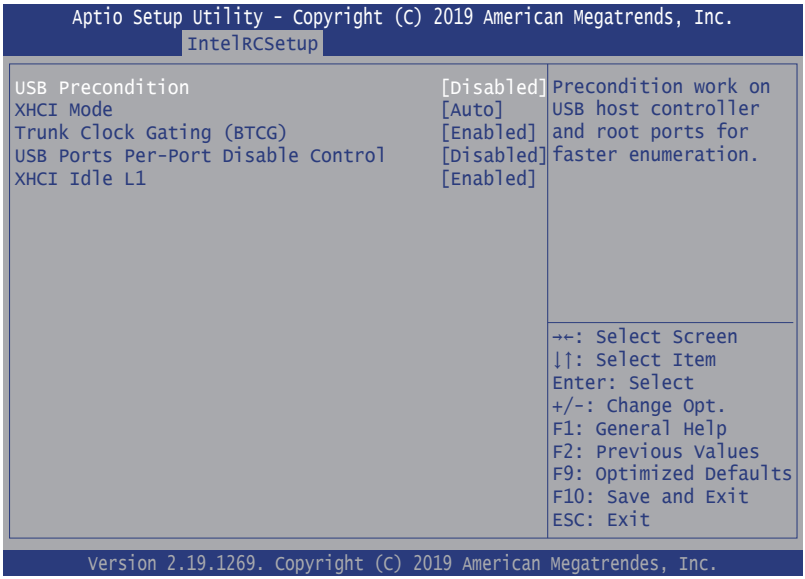
PCIe-USB Glitch W/A	**Enable** or **Disable** (default) PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG Port.
PCIe Root Port Function Swapping	**Enable** or **Disable** (default) PCIe root port function swapping feature to dynamically assin function 0 to enabled root port.
PCI Express Root Port 1~6	
PCI Express Root Port	**Enable** (default) or disable the PCI Express root port.
ASPM	Disable or set the ASPM level. Force L0s will force all inks to L0s state. “Auto” will allow BIOS to auto configure.”Disable” will disable ASPM. ► Options: **Disabled** (default), **ASPM L0s**, **ASPM L1**, **ASPM L0sL1** and **ASPM Auto**.
PCIe Speed	Select PCI Express port speed. ► Options: **Auto** (default), **Gen1** and **Gen2**

4.3.5.2 PCI SATA Configuration



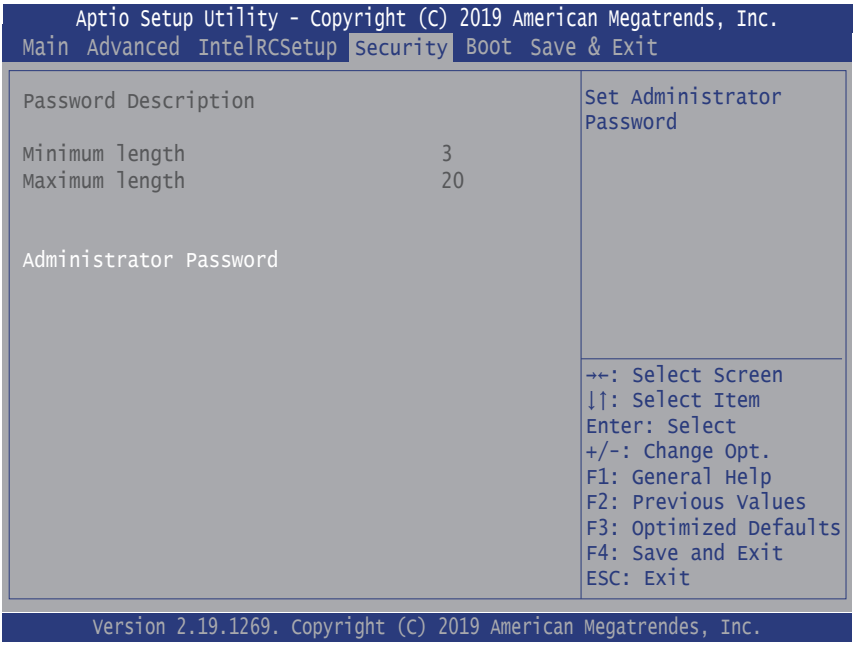
Setting	Description
SATA Controller	**Enable** (default) or **Disable** SATA controller
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive. ► Options: **Solid State Drive** (default) and **Hard Disk Drive**

4.3.5.3 USB Configuration



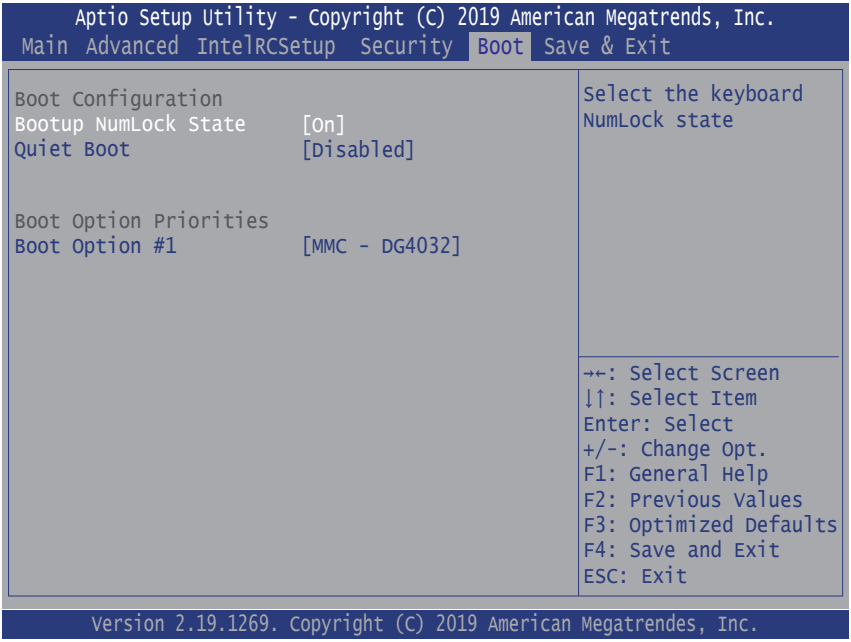
Setting	Description
USB Precondition	**Enable** or **Disable** (default) preconditoin work on USB host controller and root ports for faster enmeration.
XHCI Mode	Mode of operation of xHCI controller. ► Options: **Smart Auto**, **Auto** (default), **Enabled**, **Disabled** and **Manual**
Trunk Clock Gating (BTCG)	**Enable** (default) or **Disable** BTCG
USB Ports Per-Port Disable Control	Control each of the USB ports (0~13) disabling. ► Options: **Enabled** and **Disabled** (default)
XHCI Idle L1	**Enable** (default) or **Disable** XHCI idle L1. Enabled XHCI Idle L1. Disabled to workaround USB3 hot plug will fail after 1 hot plug removal. Please put the system to G3 for the new settings to take effect.

4.4 Security



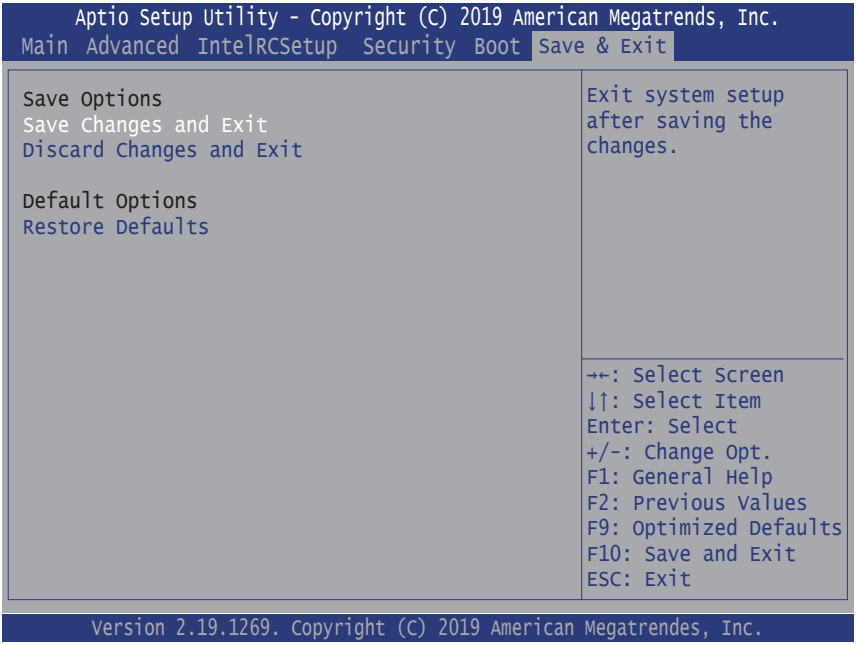
Setting	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. 2. The screen then pops up an **Create New Password** dialog. 3. Enter your desired password that is no less than 3 characters and no more than 20 characters. 4. Hit [Enter] key to submit.

4.5 Boot



Setting	Description
Boot NumLock State	Select the keyboard NumLock state. ► Options: **On** (default) and **Off**.
Fast Boot	**Enable** or **Disable** (default) boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for.BBS boot options.
Quiet Boot	**Enable** (default) or **Disable** Quiet Boot option.
Boot Option Priority	Set the system boot priorities.
Hard Drive BBS Priorities	BBS means “BIOS Boot Specification”. Sets the order of the legacy devices in this group.

4.6 Save & Exit



Setting	Description
Save Changes and Exit	Exit system setup after saving the changes. ▶ Enter the item and then a dialog box pops up: **Save configuration and exit? (Yes/ No)**
Discard Changes and Exit	Exit system setup without saving the changes. ▶ Enter the item and then a dialog box pops up: **Quit without saving? (Yes/ No)**
Restore Defaults	Restore/Load Default values for all the setup options. ▶ Enter the item and then a dialog box pops up: **Load Optimized Defaults? (Yes/ No)**
Launch EFI Shell from filesystem device	Attempts to launch EFI shell application (Shell.efi) from one of the available filesystem devices.

Appendix

Appendix A: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports. Below are the source codes written in C, please take them as WDT application example.

```
/*---------------------------------------------------------------------------*/
#include <math.h>
#include <stdio.h>
#include <dos.h>

int WDTCount;

int main(void)
{
      unsigned char                  iCount;

      printf("WDT Times ( 1 ~ 255 ) : ");
      scanf("%d",&iCount);
      printf("\n");

      WDT_Start(iCount);

      return 0;
}

void WDT_Start(int iCount)
{
      outportb(0x66,0xBA);           /* Enable Watch Dog */
      delay(2000);

      WDTCount = iCount;
      outportb(0x62, WDTCount);      /* Number is Watch Dog Down count number */
      delay(2000);

      outportb(0x62, 0x00);          /* Minute is 1 count unit by minute */
                                     /* Minute is 0 count unit by second */

}
```

```
void WDT_Stop(void)
{
      outportb(0x66,0xBB);              /* Disable Watch Dog */
}

void WDT_Clear(void)
{
      outportb(0x66,0xBA);              /* Enable Watch Dog */
      delay(2000);

      outportb(0x62, WDTCount);         /* Number is Watch Dog Down count number */
      delay(2000);

      outportb(0x62, 0x00);             /* Minute is 1 count unit by minute */
                                        /* Minute is 0 count unit by second */
}
```

Appendix B: DIO Sample Code

```
/*---------------------------------------------------------------------------*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

void GPIOMode(int iMode);
void GPIOData(int iData);
int  GPIOStatus();

int main(void)
{
    int iInput;

    GPIOMode(0xF);
    delay(10000);

    GPIOData(0x0A);
    delay(30000);
    iInput = GPIOStatus();
    printf(" Data : %2x \n",iInput);

    GPIOData(0x05);
    delay(30000);
    iInput = GPIOStatus();
    printf(" Data : %2x \n",iInput);

    return 0;
}

void GPIOMode(int iMode)
{
    outportb(0x66,0xEB);                    /* Select DIO pin to output or input */
    delay(2000);
    outportb(0x62,iMode);
}

void GPIOData(int iData)
{
    outportb(0x66,0xEA);                    /* Set DIO output pin status */
    delay(2000);
    outportb(0x62,iData);
}

int GPIOStatus()
{
    int iStatus;

    outportb(0x66,0xEC);                    /* Get DIO pin status */
    delay(2000);
     iStatus = inportb(0x62);

    return iStatus;
}
```